BREAKDOWN AND RELIABILITY OF NANOSCALE DIELECTRIC FILMS

by

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CONTENTS

LIST OF TABLES

LIST OF FIGURES

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ABSTRACT

Dielectric breakdown is the formation of a conductive path in an insulating material, and it is observed in nature (lightning strikes) and man-made equipment (spark plugs, microelectronics). In the microelectronics industry, dielectric breakdown is becoming an increasing concern for reliability engineers as device dimensions continue to shrink in order to increase computing power and speed. However, the ability to understand and predict the breakdown behavior of dielectrics in these integrated circuits is becoming more complex as new materials are introduced and the manufacturing process required to fabricate these insulators and their surrounding metal layers is constantly changing.

Due to time constraints, engineers employ a strategy to test a sample population at several high voltages in order to wear out the dielectric over time and cause failure (also called time-dependent-dielectric-breakdown). In order to extrapolate their results to low voltages and longer lifetimes, empirical models are used to fit the experimental data and then extrapolate to operating conditions. There is dispute over which empirical model provides the most accurate prediction for device lifetime, and it is most likely that a single model cannot be used to predict failure for every type of dielectric and process involved in an integrated circuit. As a result, a charge transport model was developed to provide a more comprehensive understanding of dielectric failure, in order to tie together the physical mechanism of failure to the dielectric material and the processing conditions.

The charge transport model is 1-D and incorporates current-driven and field-driven failure mechanisms. Conduction into the dielectric occurs when electrons overcome an energy barrier, and their transport throughout the dielectric depends on the electric field and the donor-type defects located in the matrix. The energetic electrons collide with the matrix, breaking bonds to increase the defect density. Breakdown occurs when a critical defect concentration accumulates, resulting in electron tunneling and the emptying of positively charged traps. The enhanced local electric field lowers the barrier for electron injection into the dielectric, causing a positive feedforward failure. The model uses a minimal number of adjustable parameters, none of which are directly used

to fit the slope of the time-to-failure versus applied electric field curve. In addition, all the parameters have some theoretical basis or have been measured experimentally.

The charge transport model is able to replicate leakage current and failure behavior for several types of dielectric materials, including low-κ SiCOH and high-κ SiN dielectrics, which are both commonly found in integrated circuits. The model can reproduce *I-V* and *I-t* curves, capturing the current decay at early stress times and the rapid current increase observed at failure for constant voltage testing. Most importantly, the model is able to predict the time-to-failure as a function of the applied electric field, without using any parameters to fit this slope. The model is able to directly compare SiCOH and SiN failure trends, and finds silicon nitride films have superior reliability due to their higher dielectric constant and deeper defect energy levels.

The model equations are refined to expand its failure prediction capabilities. The electron temperature is re-defined solely as a function of the electric field, and the defect generation rate is more closely aligned with the thermo-chemical *E* model, including a thickness dependence. The equations are also solved for in dimensionless form, which shows convection-driven electron transport, slow defect reaction kinetics, and non-uniform local field trends that depend on the thickness and density of mobile electrons in the dielectric. The refined charge transport model is able to retain all of the initial model's offerings, while also expanding its capabilities to predict dielectric failure as a function of temperature and thickness. The model replicates voltage-dependent activation energy for dielectric failure data, tying the results to the energy barrier for electron injection. Failure distributions are also replicated, based solely on dielectric spacing calculations from voltage ramp tests. The model also provides several predictions for future technology nodes as the dielectric thickness decreases. Based on the model theory, it is expected that thinner dielectrics will yield a higher dielectric strength (for planar dielectrics only) and suffer from degraded variability.

1. INTRODUCTION

The ability to predict breakdown behavior in microelectronic devices is a growing concern for reliability engineers as dimensions shrink with each new generation of devices. This section provides a basic overview of the main topics discussed in this report, including dielectric breakdown, its relevance to integrated circuits, and how continued circuit scaling, as predicted by Moore's law, is exacerbating reliability concerns relating to dielectric failure.

"Logic will get you from A to B. Imagination will take you everywhere."

-Albert Einstein

1.1 Dielectric Breakdown

In a basic definition, dielectric breakdown is the formation of a conductive path in an insulating material due to an applied electric field. Dielectric breakdown, or electrical breakdown, is observed in our lives every day. Two commonly observed examples of this phenomenon are lightning strikes and spark plugs. Lightning strikes occur in nature when gas molecules in the air are ionized by a large electric field between a cloud and an object on earth, forming a conductive path [1]. Spark plugs, commonly used in car engines and cooking grills, undergo a breakdown process similar to lightning, but on a much smaller length scale. The spark plug is designed with two electrodes approximately one millimeter apart from each other. A large voltage drop is applied across the electrodes, causing the gas molecules to ionize and break down. The high-voltage breakdown process creates a spark, resulting in combustion of the gas. In liquids, dielectric breakdown has applications for high-voltage power equipment, and the breakdown process can depend on several variables, such as metal electrode and contaminants in the liquid [2]. In gases and liquids, electrical breakdown is a reversible

Portions of this chapter have been submitted to: S. P. Ogden, Y. Xu, K. B. Yeap, T. Shen, T.-M. Lu, and J. L. Plawsky, "Charge transport model to predict dielectric breakdown as a function of voltage, temperature, and thickness," *J. Appl. Phys.*, submitted for publication.

process because the molecules forming the conduction path are able to move freely. Once the voltage is reduced or removed, the conduction path is broken as the ionized molecules dissipate.

However, for solids, the breakdown event typically results in an irreversible destruction. The earliest studies into dielectric breakdown for solid insulators were pioneered by von Hippel, Frohlich, and Zener in the 1930's. Von Hippel drew comparisons of the breakdown process in gases and liquids versus solids, discussing the ionization of the dielectric lattice as a function of the electrons' mean free path, which is strongly affected by the phase of the insulator [3]. Several studies reported the ionization of the lattice was only possible when electrons were able to gain enough energy, which occurred above a critical electric field [4]–[6]. Von Hippel also reported the importance of the electron conduction through the dielectric, characterized by an energy barrier for electron injection from the cathode, and electron trapping by defects within the dielectric [6], [7]. Later, Frohlich built upon this work by describing the conditions at which electrons obtain a stable temperature, higher than the lattice temperature [8]. These academic studies formed the backbone for all succeeding theories on dielectric breakdown, which became crucial due to the emergence of solid state electronic devices.

1.2 Integrated Circuits

Dielectric breakdown studies found practical applications in the mid-1940's and 1950's due to two major breakthroughs in electronic devices. First, the first working transistor device was developed at Bell labs in 1947 [9]. A transistor works by modulating the electronic current through a semiconductor material, and can provide an output signal larger than the input [10]. Transistors replaced vacuum tubes, substantially decreasing the amount of volume and power required for device operation. The second major transformation was the invention of the integrated circuit (IC) by John Kilby in 1958. Integrated circuits are electronic devices, such as transistors and diodes, fabricated simultaneously onto a single chip, replacing the need for discrete devices [11]. Multiple chips are also simultaneously fabricated on a single substrate, typically a silicon or silicon-based wafer. The effect of the IC was immediate and dramatic; the cost of a

transistor dropped from $45 to $2 [12]. The feature size, or relative distance between transistors (or other electronic devices) was approximately 20 μm [10].

For transistors, dielectric breakdown was a concern due to the use of an oxide material to isolate the gate metal contact from the semiconductor channel. The application of a voltage to the gate metal exerted an electric field across the oxide dielectric, resulting in the possibility of dielectric breakdown to occur. The invention of the integrated circuit created the need to electrically isolate these devices. In addition, IC's used an interconnection of metal wires and insulating materials in order to send and receive electrical signals to and from the devices. Figure 1.1 shows a schematic overview of an interconnect system in an integrated circuit, providing an electrical connection between the device level and the outside packaging. Insulators between two metal lines at different voltages are at risk to electrically break down. Dielectrics such as silicon dioxide and nitride materials have been most commonly used and studied since the emergence of integrated circuits [13].

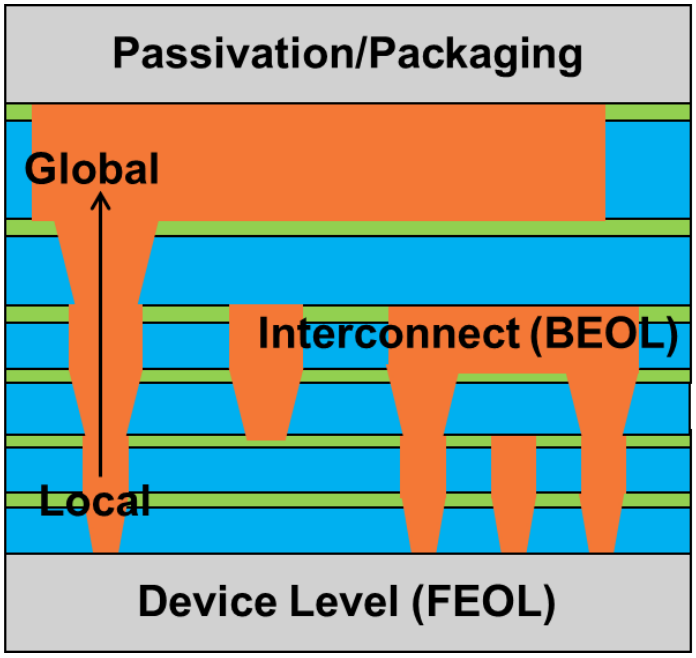

Figure 1.1. Schematic showing the interconnect structure connecting the devices to the packaging connections. Metals are represented as orange, while the dielectric materials are represented as blue and green. The metal wires width and spacing is smallest at the local levels and increase up to the global levels.

1.3 Moore's Law

The development of the integrated circuit began a revolutionary movement in the progression of electronic devices. The objective, although complex in execution, was simple in its nature: decrease the overall cost of fabrication per transistor. In 1965, Gordon Moore used existing trends to predict transistor density in a chip would double approximately every year, based on obtaining the minimum manufacturing cost per component [14]. Amazingly, this prediction held true until 1990, slowing down to doubling every 1.5 years since [12]. Moore's law derives from scaling down device dimensions based on two main process developments: improving lithography techniques and reducing defects [12], [15]. Lithography refers to the process of patterning various metals, insulators, and dopants into a silicon substrate. Projection optics have been primarily used for integrated circuits, with 193 nm imaging wavelengths being currently used [15]. Defects can refer both to intrinsic defects or foreign particles.

Device scaling has huge benefits, offering lower operating voltage and current (and therefore less power consumption), faster speed due to the increased proximity of the devices, and lower cost per transistor [14], [16]. However, one downside is that the spacing between devices is scaling faster than the voltage, causing insulating materials to operate at higher electric fields for each new technology node [17]. Thus, dielectric breakdown becomes a bigger reliability concern and larger risk for product failure.

1.4 Modern Dielectric Reliability

Device scaling led to faster speeds due to decreased signal delays through the gate. However, the shrinking dimensions caused the delay through the interconnect (RC time-delay) to increase as the resistance in the metal wires and the capacitance in the insulators both increased. By the 1990's, the delay through the interconnect, which had traditionally used silicon dioxide and aluminum, was a threat to prevent further signal speed improvement.

In order to decrease the interconnect RC time-delay, copper replaced aluminum and low-κ SiCOH materials were used as the insulation [18]–[20] at the 90 nm node (which represents the minimum feature size for the technology). However, these low-κ

materials are intrinsically weaker than SiO_2 [18] and are also more susceptible to extrinsic types of failure, such as copper ions [21], [22] and moisture absorption [23], [24]. Mature process technologies use optimized liners and barriers to prevent metal ion contamination in the dielectric, and proper passivation and processing steps for moisture absorption.

Copper and low-κ SiCOH are still being used in today's most advanced technology nodes. 14 nm feature sizes are currently in production using 300 mm wafers, as shown in Figure 1.2. 10 nm and 7 nm nodes are being developed in fab sites, with even smaller device dimensions on the horizon in the future. At these dimensions, controlling the spacing of the dielectric has become critical as lithography issues such as line overlay, via mis-alignment, and line-edge-roughness can each negatively affect the minimum spacing between wires and create enhanced electric fields which accelerate breakdown [25]–[27]. As a result, dielectric failure is now dominated by the insulator spacing for each chip [28], [29].

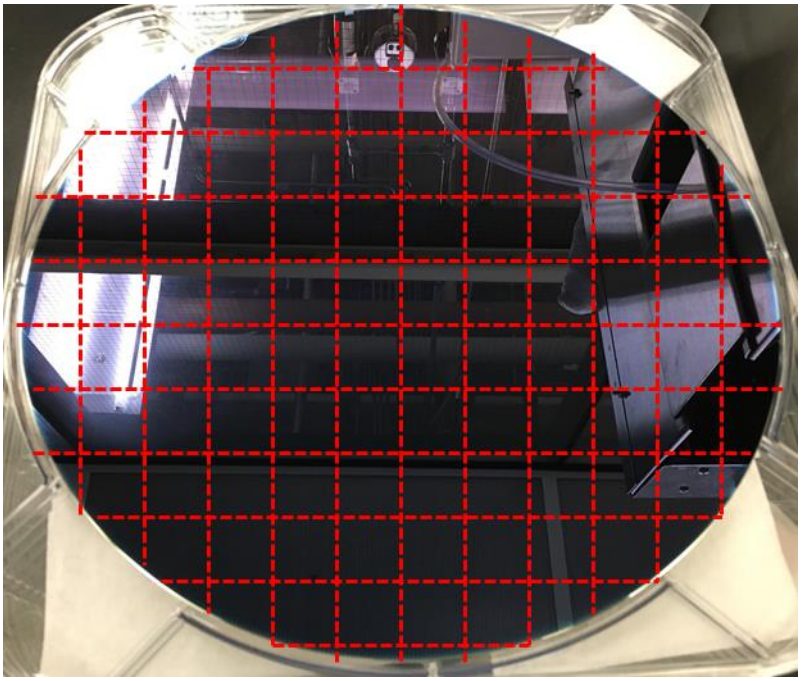

Figure 1.2. 300 mm silicon wafer, which is the same diameter as a medium pizza from DeFazio's Pizzeria in Troy, NY. Typically, 50-150 chips can be printed on a single wafer of this size, demonstrated with the dashed, red lines.

Thus, the threat of dielectric breakdown to reliability is most prevalent in the newest generations of electronic technologies, and will only continue to worsen. Dielectric materials in integrated circuits are more susceptible to contamination or damage from processing steps, which have become more numerous and complex as device fabrication becomes more challenging at each new node. In addition, trends in dielectric breakdown show insulators are subjected to higher electric fields, and are also more sensitive to process variations, which both cause reliability to degrade. It is crucial to further the understanding of the mechanism of dielectric breakdown, and identify novel approaches to improve dielectric reliability so that Moore's law can proceed uninterrupted.

1.5 Overview of Research

The work presented here focuses on the main challenges for reliability of dielectric materials, especially with relation to integrated circuits. First, the methods currently used to test and predict dielectric failure are discussed. Next, a novel model, termed the charge transport model, is proposed to predict dielectric breakdown. The charge transport model is more comprehensive than any previously proposed model, and thus, is able to provide improved insight into the breakdown process and future trends. The author concludes by proposing new ways in which the model can be employed to continue to improve the understanding of the dielectric breakdown process.

Chapter 2 discusses several important topics that relate to dielectric breakdown. For testing methodology, the various types of structures and experimental techniques used are described in detail. Electronic conduction mechanisms are introduced in this chapter, and formal equations for each type of conduction mechanism are presented. The theory and equations for various reliability models are also discussed. These models are used to extrapolate dielectric lifetime from testing conditions to operating conditions for an integrated circuit. Models are presented to scale lifetime based on voltage, temperature, and early failure populations.

Chapter 3 introduces the charge transport model, derived from previous theories on dielectric breakdown. The basic concepts of the model are discussed, and the model's equations are formally presented. The author discusses the process of determining

several model parameters from electrical data, and the significance of each parameter. Simulations are run for multiple sets of data on low-κ SiCOH and high-κ SiN, exhibiting the model's ability to predict current as a function of time or voltage, and dielectric failure as a function of voltage (for constant voltage stress) or ramp rate (ramped voltage stress). The limitations of the model are also presented, including an inaccurate prediction of failure as a function of temperature, and a lack of spacing dependence for failure (at common electric fields).

Chapter 4 addresses these model limitations by incorporating new concepts into the model's equations. The equations are also presented in dimensionless form. The new equations, both in dimension and dimensionless form, are used to predict dielectric failure trends as a function of voltage, temperature, and thickness. A novel method is also presented to verify how the dielectric thickness changes based on the location of the sample on the wafer. This method validates the model's approach to use dielectric thickness as a variable to predict failure distributions across a wafer. The model is then used to predict future trends for dielectric failure.

Chapter 5 provides the main conclusions for the charge transport model, and poses several future projects for which the model can be employed to further the understanding of dielectric breakdown in integrated circuits.

2. BACKGROUND

Dielectric breakdown has been studied extensively for more than 50 years. As a result, there is abundant literature discussing breakdown theory and trends, models developed based on the various theories, and multiple types of test structures and methodologies developed to explore dielectric failure mechanisms and behavior. This section provides a general background for the most important and relevant topics relating to dielectric breakdown. The various test structures and methodologies used to characterize dielectric materials are discussed. This section also explains the various post-testing analysis methods which are commonly used, including models to characterize the conduction mechanism and predict reliability as a function of voltage, temperature, and failure rate.

"Give me six hours to chop down a tree
and I will spend the first four sharpening the axe."
-Abraham Lincoln

2.1 Testing Methodology

The process to understand how dielectric breakdown occurs begins with the question: where does it occur? Answering this question is crucial to design the correct test structure for analysis. The next step is to then properly design the test methodology to characterize the material parameters of the dielectric material or predict the dielectric's lifetime before catastrophic breakdown occurs.

2.1.1 Test Structures

In Section 1.3, the interconnect levels in an integrated circuit were shown to consist of metal lines and vias, separated by dielectric materials. Based on design, this yields two main breakdown paths that can occur: between two metal lines without any vias, or between two metal lines with vias. The first case results in metal-metal failure, while the

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second case results in via-metal failure. To assess metal-metal dielectric failure, comb-comb structures are most commonly used. Comb-comb structures, shown in Figure 2.1, contain long metal lines, termed fingers, connected to each other by a wide metal line patterned perpendicular to the fingers (forming a comb-like pattern). Two combs can be mirrored and staggered, such that if one comb has an applied voltage while the other comb is grounded, the dielectric separating the metal fingers of each comb will be subjected to electrical stress.

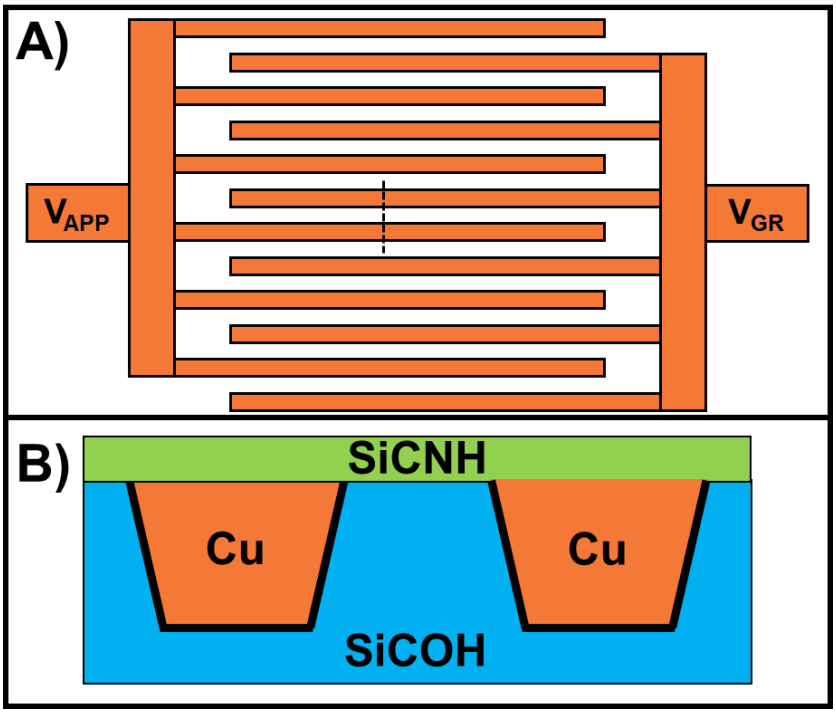

Figure 2.1. Schematic of a comb-comb structure. A) Top view showing two metal combs with a potential difference between the combs, and B) side view taken from the dashed line in the top view, showing copper lines with a sidewall angle separated by a SiCOH dielectric and passivated by a SiCNH layer covering the entire structure.

There are several advantages to using comb-comb structures to assess dielectric failure. First, these are highly dense with metal wires at different voltage potentials and common run lengths. This provides a large area (defined as the product of the number of metal fingers, the finger length, and the metal height), and mimics the layout found in integrated circuits. In fact, these structures undergo the same processing steps as

integrated circuits for fabrication. A general description of the process will be described here: a blanket dielectric film is deposited, followed by an etching of the metal trenches using lithography techniques to create the pattern. A liner/barrier metal is deposited to prevent copper contamination in the dielectric, followed by copper deposition. Excess copper is polished away to create a planar top surface. Finally, a passivation layer is deposited. The passivation layer is important to prevent moisture or other contaminants from absorbing into the dielectric or metal layers. The process overview provided here is a simplified version; there are dozens of steps to make each level in the circuit, and each step can damage the metal or dielectric. Thus, mature process technologies are required to properly assess intrinsic breakdown, although these structures are also useful for assessing and improving new technologies as the process steps are being improved. As seen in Figure 2.1B, the metal wires become thinner near the bottom of the wire, resulting in the smallest spacing (and thus highest electric field) near the top of the metal line. This minimum spacing is also dependent to the roughness of the metal lines and the overlay between the lines [25], [26].

Via chain structures are most commonly used to assess via-metal breakdown. Vias connect short metal lines on two levels creating chains (like links), as shown in Figure 2.2. Two chains connected to different pads are intertwined to create a breakdown path between a via and neighboring metal line. Via chains are fabricated using a similar scheme as comb-comb structures. Via-metal breakdown is considered to be worse than metal-metal breakdown (comb-comb) due to the addition of the via, which suffers from patterning issues such as via size uniformity and via mis-alignment in the current technology nodes [26]. The typical breakdown path in these structures can occur at the top or bottom of the via to the neighboring lower or upper metal line, depending on the design.

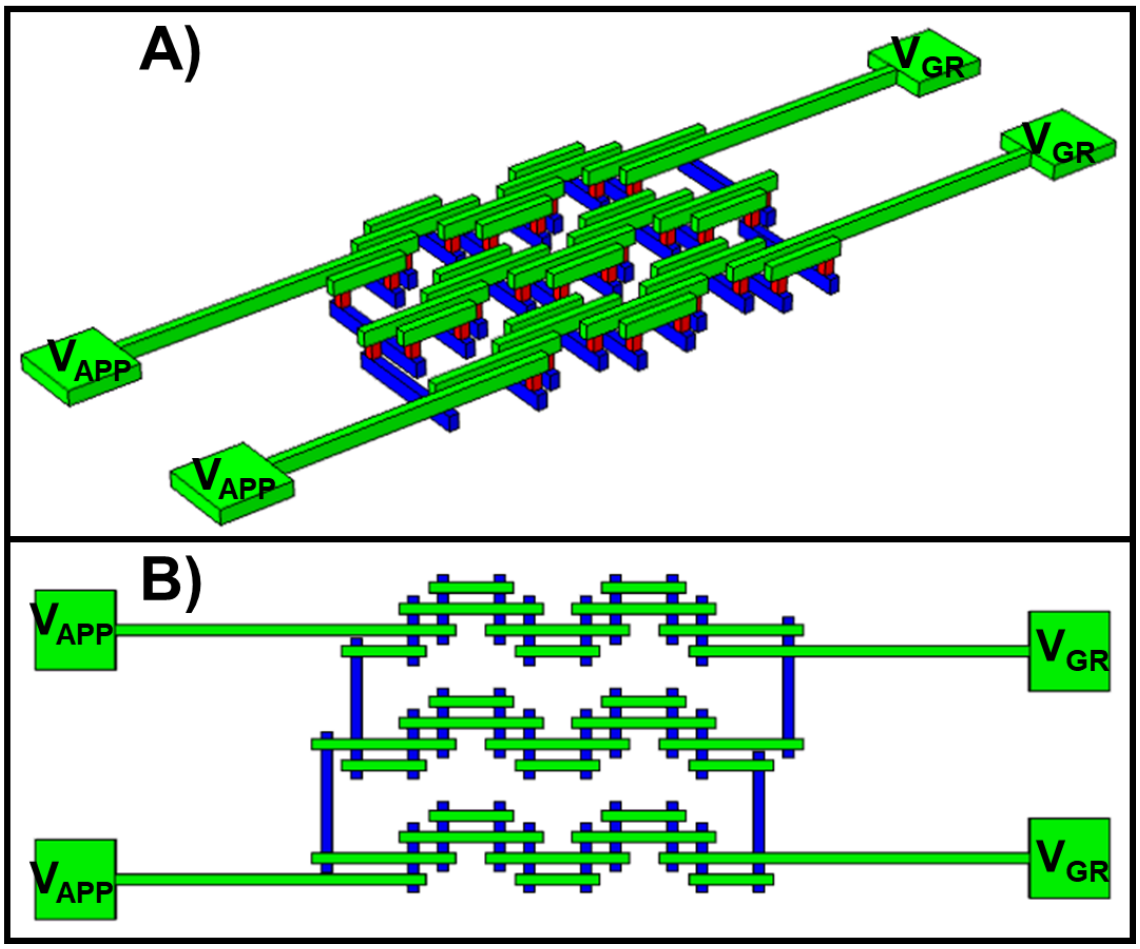

Figure 2.2. Schematic for a via chain structure. Lower (blue) and upper (green) metal lines are connected by vias (red), which are required in order to send electrical signals through different levels in an integrated circuit. The via chain structure, shown as A) angled view and B) top view, are designed to measure breakdown between a via and an adjacent metal line.

Planar structures are also often used for dielectric breakdown tests. Planar structures typically offer a simplified process scheme, such that they are used to characterize intrinsic breakdown. Figure 2.3A shows the simplest type of planar structure that can be fabricated. The dielectric material, SiCOH in this case, is grown as a blanket film on top of a silicon wafer. Metal electrodes can be separately deposited on top of the dielectric and on the back-side silicon to form contacts. If the silicon is lightly doped (usually with phosphorous or boron), a metal-insulator-semiconductor (MIS) structure is formed. MIS structures are useful to characterize the capacitance of the

dielectric. If the silicon is more heavily doped, a metal-insulator-metal (MIM) structure is formed. MIM structures can be used for dielectric breakdown characterization. Furthermore, the selection of the top electrode and the experimental conditions can be controlled to produce intrinsic breakdown or extrinsic failure due to metal ion migration [30]. One disadvantage to using blanket films is that samples are not passivated. Moisture or other contaminants can enter the dielectric through the sides of the structure, changing the dielectric breakdown physics. Samples must be carefully stored and experiments must be properly controlled to avoid contamination of the dielectric.

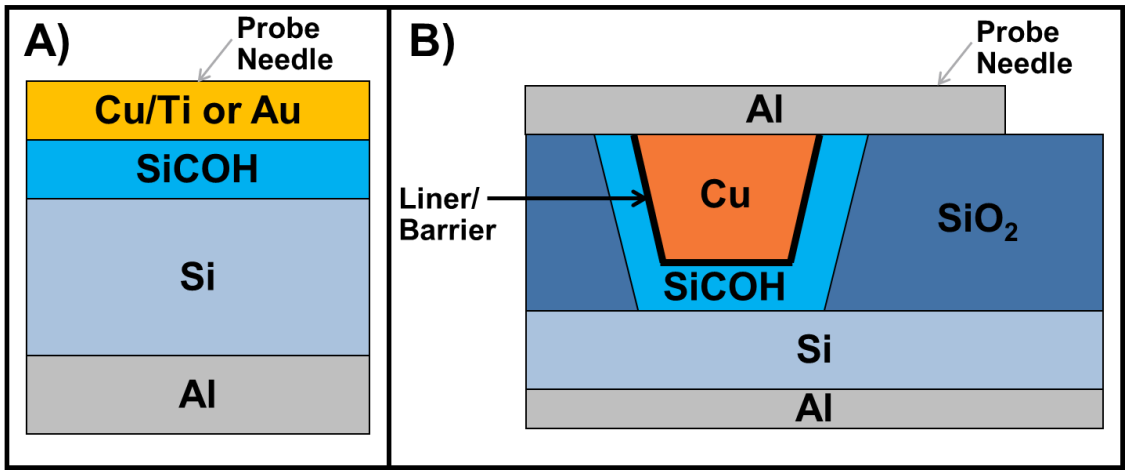

Figure 2.3. Schematics for planar structures used for dielectric testing. A) Blanket films deposited on silicon wafers; these types of samples are not passivated and susceptible to damage through the sides of the structures. B) P-cap structures deposited in silicon wafers; these types of samples are passivated and also avoid mechanical damage due to test probe needles.

Figure 2.3B shows a p-cap structure, developed at IMEC to also assess intrinsic breakdown [31]. The p-cap structure represents the middle ground between blanket planar structures and integrated structures. The fabrication process is as follows: silicon dioxide is grown on a silicon wafer, and then etched to create a trench opening. SiCOH dielectric is then grown along the bottom and sidewalls of the trench. This is followed by barrier/liner deposition, copper deposition, planarization step, and passivation [31]. Many of the process steps that are required for integrated structures are removed, resulting in a uniform, damage-free SiCOH dielectric. Further, these structures are passivated to prevent contamination, and the samples can be probed away from the area

of interest, avoiding mechanical damage issues. Therefore, p-cap structures represent an optimum approach to investigate the intrinsic breakdown properties of the dielectric. The test structure as shown is MIS due to the silicon, but a thin metallic blanket film can be deposited on top of the silicon to create a MIM structure.

2.1.2 Experimental Techniques

Dielectric breakdown testing to qualify a product for reliability purposes must be conducted under high-stress conditions due to time constraints. There are two main testing methods that are employed to characterize the dielectric material: constant voltage stress (CVS) and voltage ramp stress (RVS). In a CVS, shown in Figure 2.4, the dielectric material is subjected to a set voltage and wears out over time, known as time-dependent-dielectric-breakdown (TDDB). The leakage current through the dielectric is measured, as shown in Figure 2.4B. If the noise level of the instrument measuring the leakage current is sensitive enough for the stress conditions, information such as electron trapping and defect generation within the dielectric can be obtained before the material breaks down. Hard breakdown is typically observed, in which the current abruptly increases several orders of magnitude or higher.

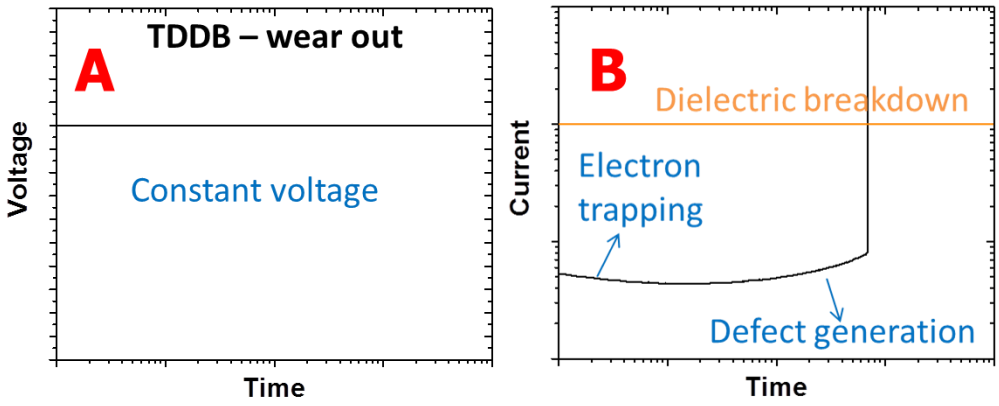

Figure 2.4. Time-dependent-dielectric-breakdown test showing A) a constant voltage applied to the dielectric, and B) the leakage current measured through the dielectric as a function of time.

The constant voltage test is more commonly used for reliability purposes. A structure is tested under several voltages, and then an empirical model is used to

extrapolate the failure time at the stress voltages to the operating conditions (see Section 2.3.1).

Although it is not standard to conduct a voltage ramp test for reliability qualification, this test can be useful to determine important material parameters. In a voltage ramp test, shown in Figure 2.5, a linearly increasing voltage is applied to the dielectric material with increasing time. The current is measured as a function of the voltage, as shown in Figure 2.5B, until the electric field exceeds the dielectric's breakdown strength and failure occurs, resulting in a current increase similarly seen in the constant voltage test. Higher ramp rates typically result in a higher breakdown voltage.

The type of conduction mechanism through the dielectric can be determined based on the shape of the *I-V* curve. The dielectric constant (κ) and the energy barrier from the Fermi level of the metal cathode to the conduction level of the dielectric (Φ_B) are determined from the *I-V* slope and magnitude of current, respectively. This will be discussed in more detail in Section 2.2. Finally, the dielectric spacing can be calculated based on the breakdown voltage if the dielectric strength, or electric field breakdown (E_{BD}), at a specific ramp rate is known, using $s=V_{BD}/E_{BD}$.

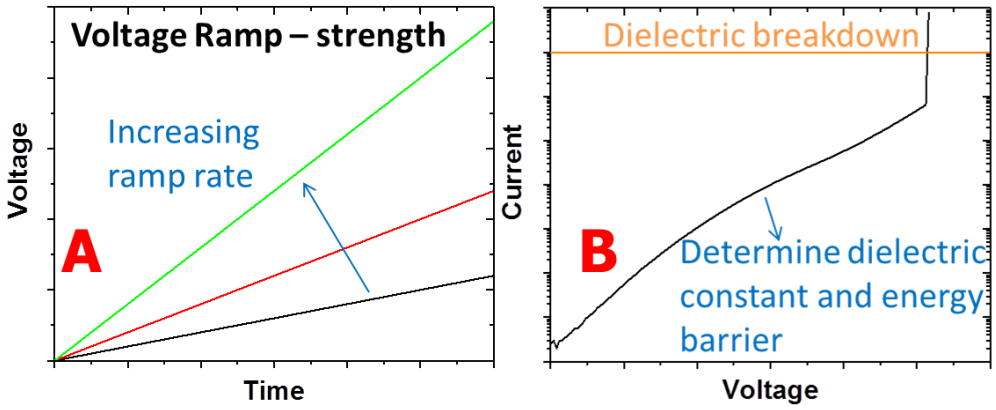

Figure 2.5. Voltage ramp test showing A) an increasing voltage as function of time, and B) the resulting current measured through the dielectric as a function of the applied voltage.

2.2 Conduction Mechanisms

Electrons in an atom form discrete energy levels, and when atoms form a solid, these energy levels split into energy bands. In these energy bands, the valence band is the highest level filled with electrons while the conduction band is the lowest energy level that is empty or partially filled with electrons [10]. For dielectric materials, there is an energy gap (typically >6 eV) between the valence band and conduction band, creating a forbidden zone through which electrons cannot exist in a perfect crystal. In reality, defects in the crystal create discrete, lower energy states which electrons can reside. A defect can be an extra atom, missing atom, dis-placed atom, or a variety of other types [12]. Although the theory describing energy levels is derived for solid crystals due to their repeating, ordered structure, these same concepts can be extended to amorphous materials as well [32]. At a contact between a metal and a dielectric, electrons must overcome an energy barrier from the Fermi level of the metal to the conduction band of the dielectric, which often limits the electronic conduction through the insulator. Therefore, this energy barrier is crucial to defining the insulating properties of a dielectric, and depends on the energy levels of the metal and dielectric, as well as several other important factors. The electron conduction through a dielectric material under stress is considered vital to predict dielectric reliability because the two concepts are believed to be strongly tied to each other. Therefore, it is crucial to understand how the electronic conduction might change as a function of voltage in order to assess dielectric lifetime.

Aside from the metal-insulator energy barrier, electronic conduction in dielectric materials can also strongly depend on defects, both intrinsic and extrinsic. Extrinsic defects can either create defects states, or produce a current if mobile. However, the three main types of conduction reported for dielectric materials all rely on electrons: Schottky emission, Poole-Frenkel conduction, and Fowler-Nordheim tunneling [33]. Figure 2.6 shows the energy level diagrams for the three types of conduction mechanism that will be explained in this section.

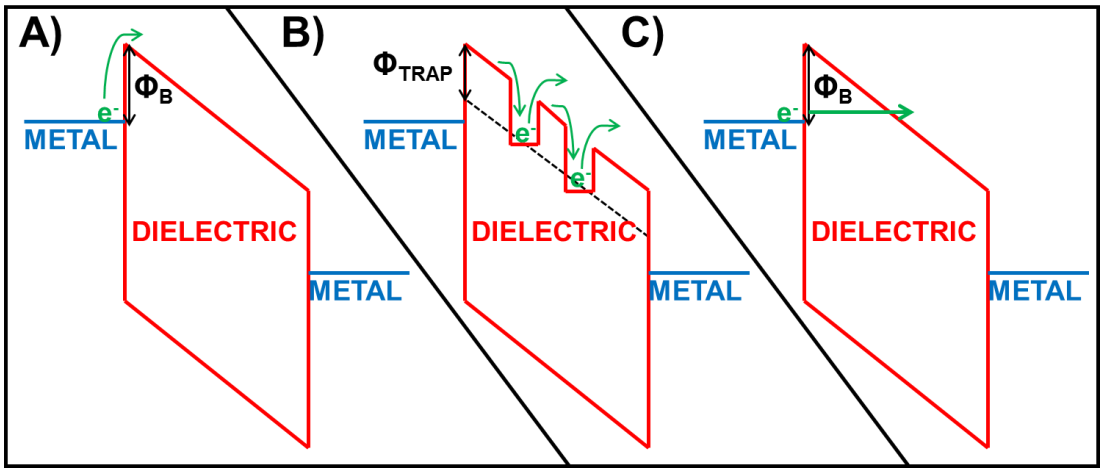

Figure 2.6. Energy level diagrams to show various conduction mechanisms in dielectric materials under stress. Blue lines represent Fermi energy levels for the metals, while top and bottom red lines represent the dielectric's conduction band and valence band, respectively. A) Schottky emission, B) Poole-Frenkel conduction, and C) Fowler-Nordheim tunneling.

Schottky emission is the most commonly reported conduction mechanism for dielectric materials [33], and has been shown to occur in SiCOH dielectric materials [34]. Figure 2.6A shows the electron injection process for Schottky emission. Electrons in the metal gain enough thermal energy to overcome the dielectric-metal energy barrier, injecting above the dielectric conduction band (where the electron is free to move through the material). Electron conduction for Schottky emission is described using:

$$J = AT^2 exp\left[\frac{-q\left(\Phi_B - \sqrt{qE/4\pi\varepsilon_\infty\varepsilon_0}\right)}{k_b T}\right], \tag{2.1}$$

where J is the current density, A is the effective Richardson constant, T is the temperature, q is the fundamental unit of charge, Φ_B is the dielectric-metal energy barrier, E is the nominal electric field, ε_∞ is the dielectric constant in the optical limit, ε_0 is the free permittivity of space, and k_b is the Boltzmann constant. Here, E refers to the nominal electric field, based on the voltage divided by the nominal thickness (V_{app}/s), where in the subsequent chapters, F refers to the localized electric field, which is a function of the location in the dielectric. The energy barrier (Φ_B) is lowered by the electric field with an $E^{1/2}$ dependence. Material parameters such as the energy barrier

(Φ_B) and dielectric constant in the optical limit (ε_0) can be calculated by plotting *ln(J)* vs. $E^{1/2}$ to obtain a linear fit.

Defect states can serve as trapping centers for electrons. Thus, for materials with a high concentration of defects, electrons are limited by their ability to conduct between traps rather than their injection into the dielectric. This is known as Poole-Frenkel conduction, shown in Figure 2.6B. Conduction occurs through the thermal activation of electrons out of defect states in the dielectric. Poole-Frenkel conduction is typically found to occur for defect-rich materials, and has been reported for both SiCOH [35] and silicon nitride [33]. It is described as:

$$J = q\mu C_{trap} E exp\left[\frac{-q\left(\Phi_{trap} - \sqrt{qE/\pi\varepsilon_\infty\varepsilon_0}\right)}{k_b T}\right], \tag{2.2}$$

where μ is the electronic drift mobility, C_{trap} is the defect density, Φ_{trap} is the defect energy level measured from the conduction band, and the other variables are the same as defined for Schottky emission. The defect energy level (Φ_{trap}) and dielectric constant in the optical limit (ε_0) can be calculated by plotting *ln(J/E)* vs. $E^{1/2}$ to obtain a linear fit. Schottky emission and Poole-Frenkel conduction are very similar, in that they depend on thermal activation of electrons over energy barriers and follow an $E^{1/2}$ dependence. These types of conduction are more favorable at high electric fields and high temperature [33].

Schottky emission and Poole-Frenkel conduction involve classical descriptions of electrons. In the classical sense, an electron cannot exist in the forbidden energy levels of the dielectric, so it must excite above those levels to enter the conduction band. Fowler-Nordheim tunneling, on the other hand, is based on a quantum mechanical approach to electronic states. Derived from Schrodinger's equation, an electron (described as a wave function) has some probability to exist on the other side of the energy barrier by a "tunneling" mechanism [33]. This works in the same way as the electron's existence in discrete energy levels; the electron is either reflected at the energy barrier or penetrates through to the conduction band. Fowler-Nordheim tunneling is described as:

$$J = \frac{q^3 E^2}{8\pi h q \Phi_B} exp\left[\frac{-8\pi\sqrt{2qm_e^*}}{3hE}\Phi_B^{3/2}\right], \quad (2.3)$$

where h is the Planck constant, m_e^* is the effective electron mass, and the remaining variables are the same as defined in the previous equations. Tunneling does not have a temperature dependence, so this type of conduction is more favorable at high electric field and low temperature. Interestingly, this equation does not have any thickness dependence directly associated with it, but Fowler-Nordheim tunneling is typically only reported for thin dielectrics less than 10 nm [33]. The energy barrier (Φ_B) and effective electron mass (m_e^*) can be calculated by plotting $ln(J/E^2)$ vs. $1/E$ to obtain a linear fit.

2.3 Reliability Models

High-voltage and high-temperature CVS tests are used to predict dielectric failure on the time scale of seconds to months, but the failure lifetime must then be projected based on the operating conditions of the product at low voltages and low temperature. The standard practice is to extrapolate the results to the operating conditions using empirical models. In addition, limited sample sizes are tested, but a small, maximum fail rate is typically allowed (~100 parts-per-million fails). Thus, empirical models are also used to extrapolate from the main population to the extreme tail for early failures.

2.3.1 Voltage Acceleration

TDDB testing is conducted at several different voltages, and then an empirical model is fitted to the experimental data and used to extrapolate to operating conditions, approximately 1 V. There have been several voltage-acceleration models that have been previously used; the E model is the most conservative while the $1/E$ model is the most optimistic.

The earliest proposed voltage-acceleration model was the E-model [36]–[38]. The E-model, or thermochemical model, attributes dielectric failure to the breakage of weak intrinsic bonds within the dielectric matrix [39]. The time-to-failure (TTF) is related to the electric field using Equation 2.4:

$$TTF = A * exp(-\gamma * E), \quad (2.4)$$

where A is a numerical constant and γ is a field acceleration parameter. The $1/E$ model, proposed by Chen et al. [40], is a current-based model. Breakdown occurs when holes are injected into the dielectric and then damage the matrix due to impact ionization [40], [41]. Equation 2.5 describes the 1/E model, given as:

$$TTF = A * exp\left(\frac{\gamma}{E}\right). \tag{2.5}$$

The power law (PL) model was originally developed for thin gate dielectrics, and proposes that breakdown occurs when hydrogen, released from the anode, damages the dielectric [42]. The power law model is represented using Equation 2.6:

$$TTF = A * E^{-n}, \tag{2.6}$$

where n is the field acceleration parameter. The power law model is the only empirical relationship for which the time-to-failure does not have an exponential relationship to the electric field.

The E-model, $1/E$ model, and PL model were designed to predict intrinsic, or electronic, failure in dielectric materials. However, the introduction of porous dielectric films and copper metal wires in IC interconnects led to new, extrinsic failure modes. The $\sqrt{E}$-model, originally proposed by Allers et al. [43], was modified to also predict copper-induced failure [34], [35]. In this model, the presence of copper ions leads to the $\sqrt{E}$-dependent conduction mechanisms of Poole-Frenkel or Schottky emission [34], [35]. Equation 2.7 describes the $\sqrt{E}$ model as:

$$TTF = A * exp\left(-\gamma * E^{\frac{1}{2}}\right). \tag{2.7}$$

The lucky electron (LE) model, or impact damage model, was proposed by Lloyd et al. [44], and was modified to include a copper component [45]. This model combines the $1/E$ model and $\sqrt{E}$-model, and is based on the probability that an electron, accelerated by the electric field, will have sufficient momentum to damage the dielectric and cause breakdown [44], [46]. The lucky electron model has an extra fitting parameter compared to the previously described lifetime models, and is represented by Equation 2.8:

$$TTF = \left(\frac{A}{E}\right) * exp\left(-\gamma * E^{\frac{1}{2}} + \frac{\alpha}{E}\right), \tag{2.8}$$

where γ and α are the two field-acceleration parameters.

Reliability engineers have commonly used these models to predict lifetime, but there is still dispute over which model most accurately predicts device failure under operating conditions. Figure 2.7 shows experimental failure data over a wide range of electric fields, and the corresponding fits to the five empirical models described above. It is difficult to distinguish which model provides the best fit to the data, and mathematical analysis to analyze the best fit can be deceptive due to the uncertainty associated with the data set. However, the proper model selection is important because at low fields where products operate, the models deviate and predict lifetimes that vary over orders of magnitude.

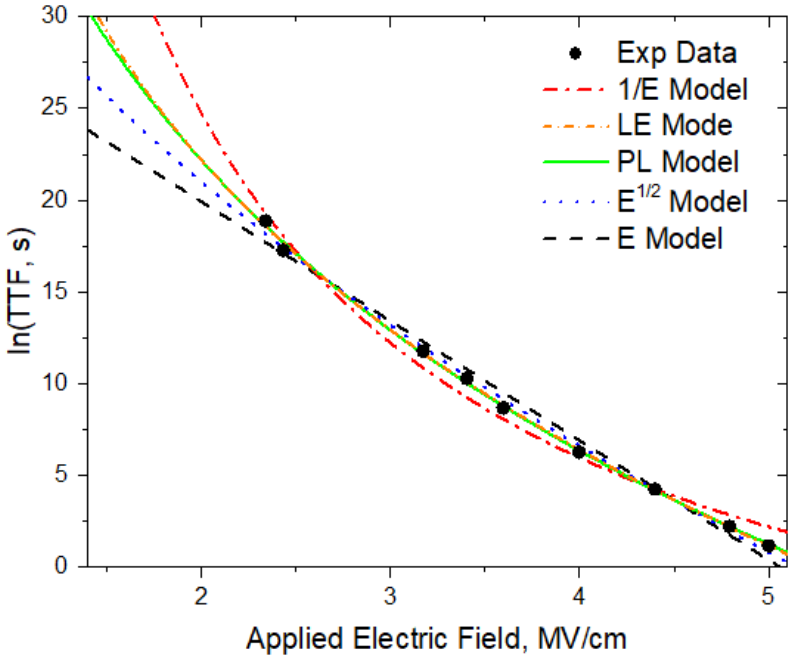

Figure 2.7. Dielectric failure data (black circles) and the corresponding fits by the empirical lifetime models. Most models can fit well to experimental data, but provide drastically different lifetime projections at low-field operating conditions. Experimental data obtained from [47].

A shortcoming of these single equation, algebraic, models is the drastic simplification of the complex mechanisms involved in dielectric breakdown. The constants used in these models to fit the data are at best, only loosely tied to the physical mechanisms, materials, and processes used to generate the data. Therefore, a more

comprehensive model built primarily on theoretical considerations could offer an improved insight toward these variables' effect on dielectric behavior. Haase et al. [48] recognized this issue, and proposed a set of nonlinear partial differential equations to describe the conduction of charge carriers in the dielectric and the formation of defects which lead to failure. However, Haase's model fails to replicate the large instability in electronic conduction at failure, usually seen as a sharp increase in leakage current and so could not be used to describe dielectric breakdown as a function of applied field and temperature.

2.3.2 Temperature Dependence

At first glance, temperature acceleration for dielectric failure appears more straightforward than voltage acceleration. It is standard practice to use the Arrhenius relationship to extrapolate failure from testing conditions to operating conditions, given as:

$$ln(TTF) = ln(A) - \frac{E_{act}}{k_b T}, \tag{2.18}$$

where *TTF* is the time-to-failure, *A* is a pre-exponential constant, E_{act} is the TTF activation energy, k_b is the Boltzmann constant, and *T* is the test temperature. *A* and E_{act} are the two fitting parameters to the experimental data. This equation implies E_{act} is a constant. However, studies over the past 30 years have consistently shown that the activation energy increases as the test voltage decreases [49]–[52]. As a result, fail rates from dielectric breakdown are over-estimated for chips that operate at lower temperatures than testing conditions. To offset this, tests can be conducted at the same temperature at which the product operates. However, this can lead to increased testing resources for a company fabricating multiple products which operate at different temperatures.

2.3.3 Failure Distributions

Wafer sizes have increased over the years, and presently, state-of-the-art fabrication facilities use wafers with a diameter of 300 mm. Many structures are deposited over the entire surface of the wafer, whether it is the integrated chip for a customer product, or a

test vehicle designed to isolate failure to a certain location for reliability qualification. The dielectric thickness isolating adjacent metal wires is on the length scale of tens of nanometers, and as a result, process variations across the wafer have become a huge concern for reliability [53]. Disparities in the dielectric spacing, such as line-edge-roughness (LER), line-to-line overlay, and via-to-line misalignments, are the most prevalent process variations [54], but there are other parameter variations as well, such as defect concentrations and barrier thickness. The summation of these process variations across the entire wafer lead to samples that fail at different times despite being subjected to the same stress conditions.

Two of the most common distribution functions used for failure analysis are the log-normal distribution and Weibull distribution. Log-normal distributions are typically associated with gradual degradation of the material (such as mass diffusion), while Weibull distributions better describe weak-link failure [12]. Dielectric breakdown is widely described as a weak-link failure, and thus dielectric failure rates are modeled using the Weibull distribution, given as:

$$CDF = 1 - exp\left[-\left(\frac{TTF}{t_{63\%}}\right)^{\beta}\right], \tag{2.10}$$

where CDF is the cumulative distribution function (or cumulative failure probability), $t_{63\%}$ is the scale parameter, and β is the shape parameter. Simply put, $t_{63\%}$ indicates the average time at which a sample will fail, while β represents the variation in the sample population. Figure 2.8 shows a failure distribution plot where the samples have the same scale parameter ($t_{63\%}$), but different values of β. The importance of process variation control becomes evident from this graph. At operating conditions, the customer product must meet criteria of a maximum number of failures per population size, usually given in parts-per-million. If process variation is large, the early sample fails will occur at a much lower lifetime than a sample population with a tightly controlled process. Weibull distributions can be plotted on a linear scale by transforming Equation 2.10 into:

$$\ln[-\ln(1 - CDF)] = \beta \ln(TTF) - \beta \ln(t_{63\%}), \tag{2.11}$$

where β can be calculated from the slope and $t_{63\%}$ can be calculated from the y-intercept once β is known.

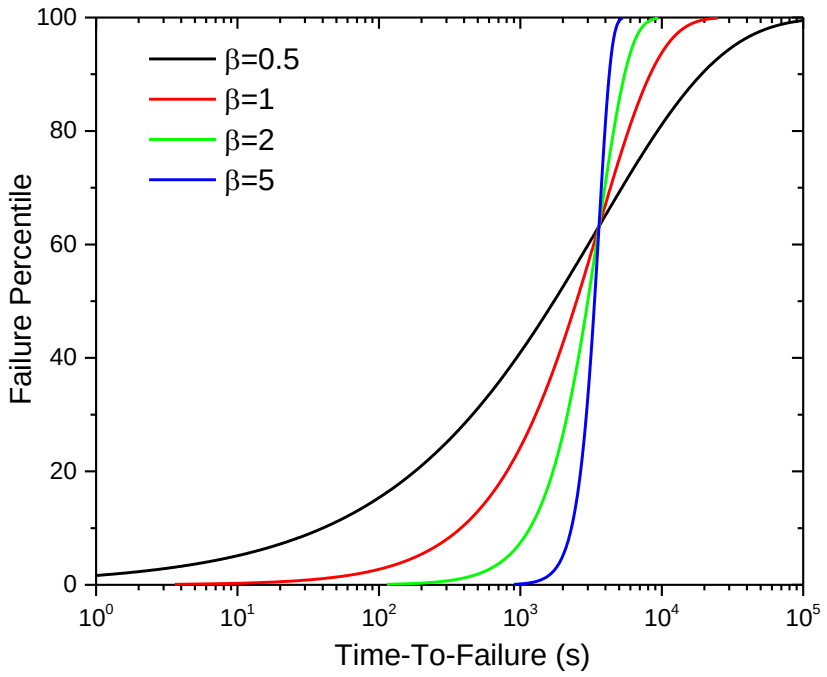

Figure 2.8. Distribution plot showing samples with the same t_{63} (λ=3600 s), but different distribution scales (β).

It is essential to accurately predict the failure distribution, especially as dielectric breakdown becomes more difficult to qualify for new technology nodes. However, the accuracy of a statistical approach, such as a Weibull distribution, is dependent on the sample size. In addition, domination of spacing variation and other process concerns are beginning to threaten the applicability of the Weibull distribution for advanced technology nodes [55], [56]. Figure 2.9 shows experimental data with a large number of samples for each voltage (>100), and the corresponding fits to the log-normal distribution and Weibull distribution. The data originates from the same wafer, but early failures at 14 V appear to fit the log-normal prediction more accurately while the early failures at 13 V appear to fit the Weibull distribution more accurately. This seemingly contradictory finding perfectly exemplifies the disadvantage to using statistical models; these fitting models cannot tie the processing conditions or fundamental electrical data to the failure results.

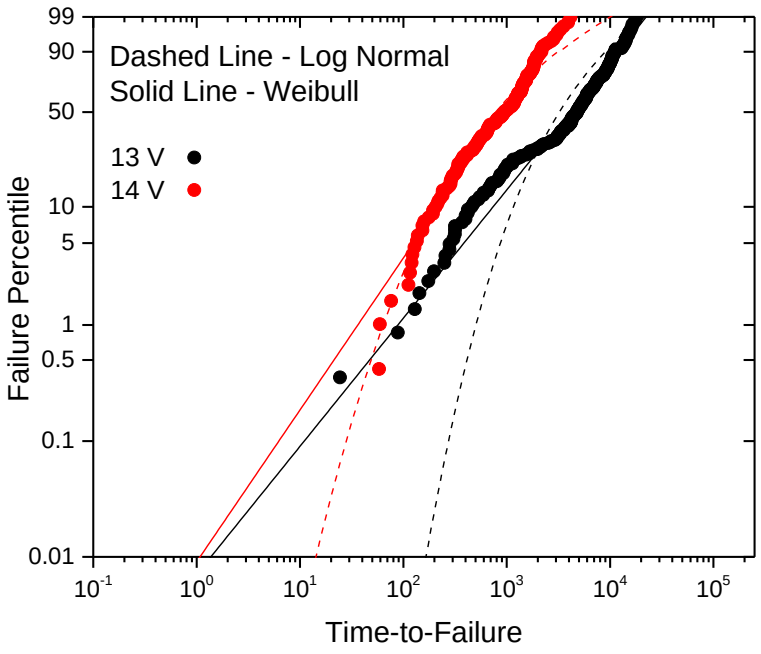

Figure 2.9. Experimental failure distributions at 13 V and 14 V. The data is from the same wafer, but different voltages appear to follow different failure distribution models.

3. CHARGE TRANSPORT MODEL

The use of statistical analysis to evaluate dielectric failure at low operating voltages and early fail rates has several disadvantages. Therefore, a more comprehensive model that can both predict failure and provide a more theoretical understanding of dielectric behavior is crucial for reliability assessment. In this section, a charge transport model is presented to predict intrinsic reliability for dielectric materials. The section includes the model's concepts, assumptions, equations, and boundary/initial conditions. Simulation results are compared to multiple sets of data, including two types of dielectric materials (low-κ SiCOH and high-κ SiN). Finally, the limitations of the model are addressed.

"With four parameters I can fit an elephant,
and with five I can make him wiggle his trunk."
-John von Neumann

3.1 Failure Theory and Assumptions

Electrons are injected into the dielectric over an energy barrier, and are able to move freely through the dielectric if their energy is greater than the conduction band. Before stress or during the early periods of testing, there are a few intrinsic defects present, and these defects can serve to trap the mobile electrons. Figure 3.1A shows a schematic of the electron conduction through the dielectric at the early stages of electrical stress. The schematic is for a metal-insulator-metal structure, where electrons are injected above the conduction band of the dielectric from the Fermi level of the metal electrode. Intrinsic failure originates from the interaction of high energy electrons with the dielectric matrix. The electrons gain energy due to the applied electric field, and lose energy to the matrix through collisions with defects or other constituents of the dielectric [57], [58]. The

Portions of this chapter appeared in: S. P. Ogden, J. Borja, J. L. Plawsky, T.-M. Lu, K. B. Yeap, and W. N. Gill, "Charge transport model to predict intrinsic reliability for dielectric materials," *J. Appl. Phys.*, vol. 118, no. 12, Sep. 2015, Art. no. 124102.
Portions of this chapter appeared in: S. P. Ogden, T.-M. Lu, and J. L. Plawsky, "Electron transport and dielectric breakdown in silicon nitride using a charge transport model," *Appl. Phys. Lett.*, vol. 109, no. 15, Oct. 2016, Art. no. 152904.

energy released during the collisions becomes available to generate additional defects, and the mobile electrons become trapped within the dielectric by these defects. As the defect concentration increases over time, the probability for trapped electrons to tunnel from trap-to-trap through the dielectric increases. This trap-assisted tunneling is quickly accelerated once a critical defect concentration is reached [59]. Figure 3.1B shows a schematic of the electron conduction near failure of the dielectric, including the additional conduction mechanism of trap-to-trap tunneling. The emptying of traps due to tunneling electrons enhances the local field at the cathode. This causes an increase in the injection of electrons, and further increases defect generation. This is known as positive feedback, or feed-forward, failure [40], [60], and is the cause for the abrupt increase in current seen at failure.

The model includes the following simplifying assumptions.

1. The leakage current is directly related to a mobile electron flux. Only current due to electron flow is considered at this time.
2. Mobile electrons gain energy and are accelerated by the applied and local electric fields. Electrons lose energy due to scattering by traps and the substrate, and this energy becomes available to generate new defects.
3. Defects and trapped electrons are in thermal equilibrium with the substrate.
4. All traps have a positive charge, and serve to enhance the local field near the cathode within the dielectric.
5. Electron conduction near failure is supported by direct trap-to-trap tunneling.

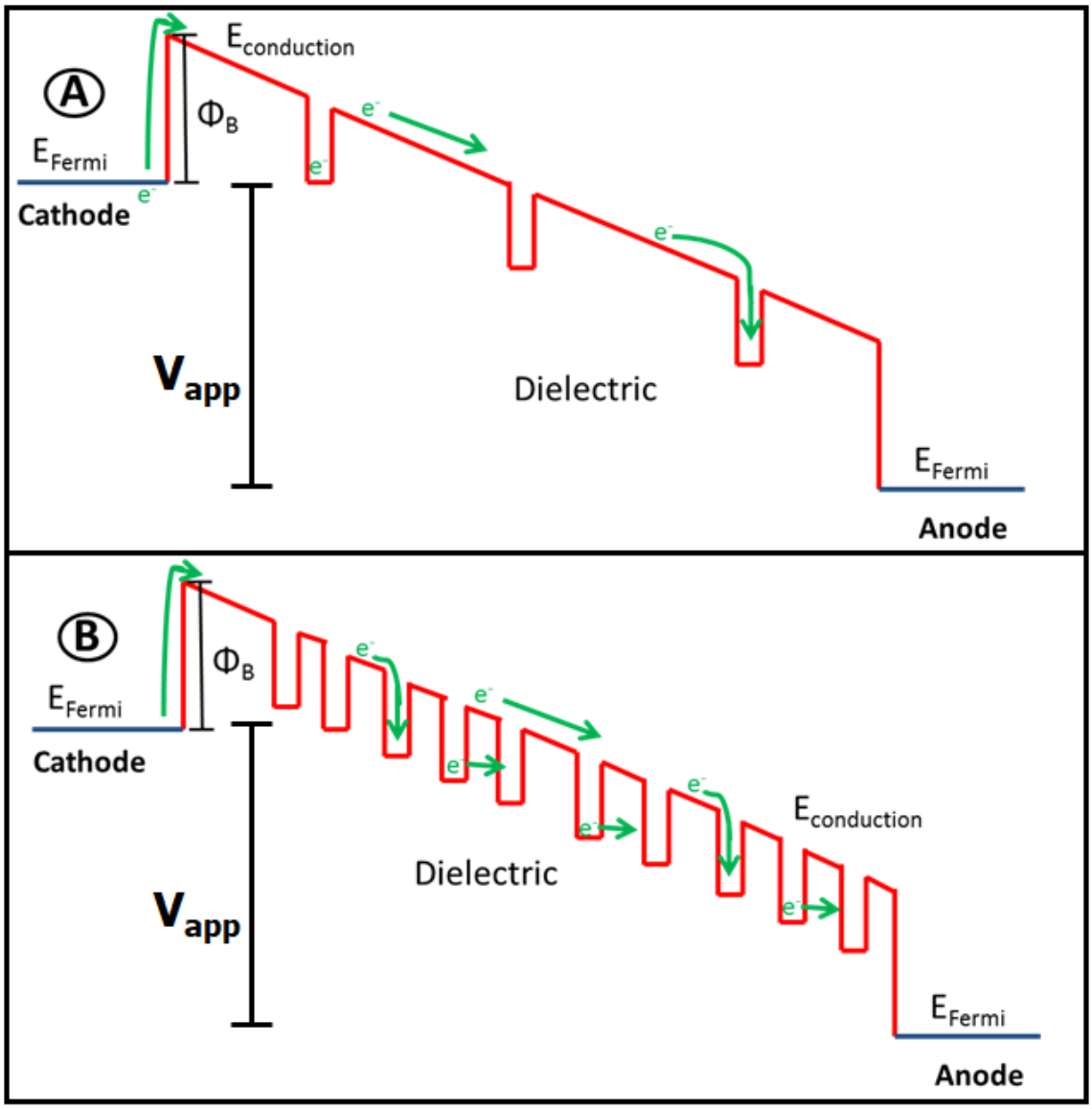

Figure 3.1. Energy level schematics to illustrate the electron conduction through the dielectric subjected to electrical stress at A) early stress times and B) near dielectric failure. There is an additional trap-to-trap tunneling conduction mechanism as the dielectric is near failure due to the accumulation of defects.

3.2 Model Equations

The charge transport model is comprised of a set of nonlinear, time-dependent, partial differential equations. The potential distribution and the local electric field, $F =$

$-\partial V/\partial x$, are affected by the accumulation of charge in the dielectric, and obey Poisson's Equation:

$$\frac{\partial^2 V}{\partial x^2} = \frac{q}{\kappa \varepsilon_0}\left(C_{trap} - C_{e,mob,total} - C_{e,trapped}\right), \tag{2.1}$$

where q is the fundamental unit of charge, such that $q < 0$, ε_0 is the vacuum permittivity, and κ is the dielectric constant. Overall, the dielectric is nearly neutral, but the buildup of charge affects the local electric field. The accumulation of positive charge enhances the field at the cathode, while a net negative charge reduces the field at the cathode. C_{trap} is the concentration of traps in the dielectric. Traps, or defects, are assumed to be donor-like in nature, and therefore have a positive charge [61], [62].

Electrons are defined as either mobile ($C_{e,mob,total}$) or trapped in the dielectric ($C_{e,trapped}$). Their continuity equations are expressed as:

$$\frac{\partial C_{e,mob,total}}{\partial t} + \frac{\partial}{\partial x}\left(J_{e,mob,total}\right) = g_{e,tunnel} - \frac{\partial C_{trap}}{\partial t} \tag{2.2}$$

and

$$\frac{\partial C_{e,trapped}}{\partial t} = \frac{\partial C_{trap}}{\partial t} - g_{e,tunnel}, \tag{2.3}$$

where

$$J_{e,mob,total} = v_e C_{e,mob,total} - D_e \frac{\partial C_{e,mobile}}{\partial x}. \tag{2.2a}$$

There are two types of mobile electrons: $C_{e,mobile}$ refers to thermally excited electrons traveling above the conduction band in the dielectric, and $C_{e,tunnel}$ represents electrons that tunnel directly between adjacent traps, such that $C_{e,mob,total} = C_{e,mobile} + C_{e,tunnel}$. The mobile electron flux through the dielectric is represented as $J_{e,mob,total}$. Both thermally excited electrons and tunneling electrons have drift components in the flux term, but tunneling electrons are not able to diffuse through the dielectric. Trapped electrons are immobile in the dielectric. The electron velocity and diffusion coefficient are defined as:

$$v_e = \frac{qF}{|qF|}\left(\sqrt{\frac{|qF\lambda_{trap}|}{m_e^*}} + \sqrt{\frac{8k_bT}{\pi m_e^*}}\right) \tag{2.4}$$

and

$$D_e = \lambda_{trap}\sqrt{\frac{k_b T}{3m_e^*}}, \tag{2.5}$$

where m_e^* is the effective electron mass, k_b is the Boltzmann constant, T is the substrate temperature, and λ_{trap} is the scattering length. The average electron velocity is represented using energy gained from the electric field, as well as a thermal energy component. Electrons gain energy from the field, and travel in a ballistic motion until they are scattered by a defect in the dielectric. The electron velocity is in the opposite direction to the local field. The diffusion coefficient is obtained assuming that the scattering time is independent of the field [63].

The scattering length is based on a Debye length [64]:

$$\lambda_{trap} = \left(\frac{\kappa\varepsilon_0 k_b T}{q^2 C_{trap}}\right)^{1/2}. \tag{2.6}$$

The scattering length is inversely proportional to the square root of the trap concentration, and represents the distance beyond which electrons are unaware of other charges, such as defects or trapped electrons.

Electrons are trapped in the dielectric at the same rate that defects are generated, which is to say that every time a defect is created, that defect immediately traps an electron. Electrons trapped in the dielectric can gain mobility by tunneling through the dielectric trap-to-trap. The rate at which tunneling electrons are generated is derived as:

$$g_{e,tunnel} = \frac{\partial}{\partial t}\left[C_{e,trapped} exp\left(-\frac{4\sqrt{2m_e^*}}{3\hbar|qF|}\Phi_{trap,eff}\right)\right], \tag{2.7}$$

where $\hbar$ is the reduced Planck constant. The tunneling electron generation rate is proportional to the concentration of electrons trapped in the dielectric. It is also proportional to the WKB tunneling probability, represented as the exponential function in Equation 2.7. The trapped electrons must overcome an effective energy barrier to escape the trap in which they are confined. This effective energy barrier is defined as:

$$\Phi_{trap,eff} = \Phi_{trap}^{3/2} - \left(\Phi_{trap} - \left|qF\lambda_{trap}\right|\right)^{\frac{3}{2}}, \tag{2.7a}$$

where Φ_{trap} is the generic barrier height for traps, as measured from the conduction band. As the defect concentration increases and thus, the scattering length decreases, the probability for trapped electrons to tunnel through the dielectric increases.

The rate of defect generation is expressed as a second order chemical reaction between the mobile electrons and the dielectric matrix.

$$\frac{\partial C_{trap}}{\partial t} = \left(\frac{v_e}{\lambda_{trap}} C_{e,mob,total}\right)\left(\frac{C_{trap,max} - C_{trap}}{C_{trap,max}}\right) exp\left(\frac{\Delta H_{,eff}}{k_b T_e}\right). \quad (2.8)$$

Electron diffusion is assumed to have a negligible effect on trap creation such that only the electron's drift component is included in the generation term. A self-limiting reaction mechanism is included based on the maximum number of available trap sites, denoted as $C_{trap,max}$. For a silica-based dielectric, the maximum number of traps is based on the number of fundamental silicon units, such as silica tetrahedra, comprising the dielectric. Traps are confined to the matrix, and only have a generation term because their creation is irreversible. The activation energy for defect formation (ΔH), a constant parameter, is offset by the magnitude of the local electric field, defined as an effective activation energy:

$$\Delta H_{eff} = \Delta H - \beta_{PF} F_{polar}^{\frac{1}{2}}, \quad (2.8a)$$

where

$$\beta_{PF} = \sqrt{\frac{q^3}{\pi \kappa \varepsilon_0}} \quad (2.8b)$$

and

$$F_{polar} = \left(\frac{2 + \kappa}{3}\right) F. \quad (2.8c)$$

The ionization energy for a single coulombic potential well is lowered by $\beta_{PF} F_{polar}^{1/2}$ at a distance equal to the Poole-Frenkel radius [65]. The polarized field, F_{polar}, is used in lieu of the local field because polar bonds stretch and compress due to the electric field, resulting in weaker bonds which are more easily broken [66]. The polarized electric field is expressed using Equation 2.8c, known as the Lorentz Relation [66].

The electron temperature is not in equilibrium with the substrate temperature, and also plays a role in generating traps. The electron temperature [58] is defined as:

$$T_e = T\left[1 + 5.14\left(\frac{F\lambda_{trap}}{\hbar\omega_0}\right)^2\right]. \quad (2.8d)$$

Electrons gain energy from the field, and lose energy to scattering due to acoustic phonons. The energy lost by electrons to phonons is denoted as $\hbar\omega_0 = 4.0$ eV [67]. As the scattering length decreases, electrons in the dielectric are unable to gain significant energy from the electric field, and the electron temperature approaches the substrate temperature.

3.3 Boundary Conditions and Initial Conditions

This model can be solved in one dimension with the use of boundary conditions and initial conditions for Poisson's Equation and the continuity equations for mobile electrons, trapped electrons, and traps. The cathode is defined as $x = 0$ and the anode is defined as $x = s$, where s is the dielectric thickness. The boundary conditions for the voltage are given as:

$$V(x = 0, t) = 0, \quad (2.9)$$

$$V(x = s, t) = V_{app} \quad (2.10a)$$

or

$$V(x = s, t) = R * t. \quad (2.10b)$$

The cathode is grounded while the voltage applied to the anode can either be a constant voltage (V_{app}), as given in Equation 2.10a, or a ramped voltage, as given in Equation 2.10b. In this equation, R is the ramp rate, in units of V/s, and t is the time, in seconds. The boundary conditions for the mobile electrons are defined as:

$$C_{e,mob,total}(x = 0, t) = N_{e,metal}\left[exp\left(-\frac{\Phi_{B,eff}}{k_b T}\right)\right], \quad (2.11)$$

where

$$\Phi_{B,eff} = \Phi_B - \left(\frac{|Fq^3|}{\pi\varepsilon_\infty\varepsilon_0}\right)^{\frac{1}{2}}, \quad (2.11a)$$

and

$$C_{e,mob,total}(x = s, t) = 0, \quad (2.12)$$

where ε_∞ is the dielectric constant in the optical limit. Electrons are injected into the dielectric at the cathode through a modified Schottky conduction mechanism. The electrons in the metal must overcome an energy barrier, Φ_B, to enter the dielectric. This energy barrier is lowered by the applied field with a $F^{1/2}$ dependence seen in Schottky emission or Poole-Frenkel conduction. The concentration of electrons at the cathode, $N_{e,metal}$, is assumed to be 8.5×10^{28} m^{-3}, based on one electron per copper atom [68]. The concentration of electrons is set equal to zero at the anode assuming that all the electrons reaching the anode escape the dielectric. This leads to the maximum electron current. The initial conditions are specified as:

$$C_{e,mob,total}(x, t = 0) = 0, \tag{2.13}$$

$$C_{e,trapped}(x, t = 0) = 0, \tag{2.14}$$

and

$$C_{trap}(x, t = 0) = C_{trap,0}. \tag{2.15}$$

Initially, there are no mobile or trapped electrons in the dielectric, but there are defects present.

The set of non-linear partial differential equations is solved using COMSOL, a finite-element based modeling software. However, alternate commercial or home-made software can be used as well. The last equation converts the mobile electron flux into a leakage current or current density, depending on how the electrical data is presented. The leakage current through the dielectric is related to the mobile electron flux using:

$$I = qA_{eff}J_{e,mob,tot}, \tag{2.16a}$$

where A_{eff} is the effective area for electronic conduction. This equation is used for the SiCOH data presented in this chapter, which was reported as leakage current. However, the silicon nitride data obtained from Allers [43] provided leakage current density, which can instead be represented as:

$$J = qP_{eff}J_{e,mob,total} \tag{2.16b}$$

where J is the current density and P_{eff} is defined as the trapping fraction. Conduction does not occur uniformly across the entire dielectric area, but through weak paths in the dielectric where conduction is promoted by a lower energy barrier or larger defect density. Failure occurs when the defect density through one of these paths reaches a

critical concentration and the path becomes conductive. Therefore, P_{eff} can also be described as the fraction of the dielectric which electrons conduct through defects. P_{eff} is proportional to the total number of weak paths through which conduction occurs, as well as the cross-sectional area of the traps. Relating (2.16a) and (2.16b) yields:

$$A_{eff} = A * P_{eff} \tag{2.16c}$$

where A is the test structure dielectric area. This establishes the relationship between the parameters used to calculate either the current (A_{eff}) or current density (P_{eff}). The charge transport model replicates conduction and failure through the weak spots in the dielectric, and therefore, A_{eff} is proportional to the test structure dielectric area as well as the fraction of the dielectric through which conduction occurs. P_{eff} could not be calculated for the low-κ SiCOH samples because the test area was not given, but this parameter can be determined for these Si_3N_4 results because the conduction data was published as current density instead of current. P_{eff} was previously reported to be ~10^{-8} based on charge-to-breakdown calculations for a Si_3N_4 dielectric [69]. This number indicates that conduction only occurs through a very small fraction of the dielectric area (one part in 100 million).

3.4 Simulation Results

In this section the preliminary results of the charge transport model are presented, as applied to various dielectric materials. The section includes current vs. voltage, current vs. time, and time-to-failure vs. electric field results for several low-κ SiCOH dielectrics and a high-κ SiN dielectric material.

3.4.1 Low-κ SiCOH

Integrated circuit interconnects serve as the communication network between the transistor devices and external command, and consist of copper metal wires isolated by a dielectric material. SiO_2 was originally used as the insulator, but was replaced by a low-κ SiCOH material in 2001 in order to reduce signal delay, power consumption, and cross-talk noise [53], [70]. However, SiCOH has a lower breakdown strength than SiO_2 [71], and due to its porosity, is susceptible to several other failure mechanisms due to

copper ions [21], [22] and moisture contamination [23], [24]. Therefore, its reliability is a huge concern for integrated circuits.

Simulations were run for comparison to experimental data on low-κ SiCOH obtained from three independent sources. Low-field reliability testing data were extracted from test structures reported in papers by Chery et al. [47] and Croes et al. [72]. In addition, high-field tests were conducted at GLOBALFOUNDRIES (GF) on comb-comb test structures. For each data set, the dielectric constant (κ) for the SiCOH dielectric is 2.5 and the dielectric constant in the optical limit (ε_∞) is calculated to be 2.0 [73]. The initial defect density is defined as $C_{trap,0}$ = 2x10^{23} m^{-3} [74]. These as-grown donor-type traps are positive in nature [61], and can most likely be attributed to carbon dangling bonds due to carbon residues left in the film by the incomplete removal of porogen [74], [75]. The energy barrier for the main defect affecting conduction was measured to be Φ_{trap}=1.2 eV [20]. The effective mass of the electron is defined as 0.5m_e, based on SiO_2 [76], where m_e is the mass of a free electron. Table 3.1 shows a summary of material parameters used in the simulations.

Table 3.1. Parameters used in all low-κ SiCOH simulations, based on the given reference.

Parameter	Value	Source
$C_{trap,max}$	1.0 x 10^{29} m^{-3}	Calculated
$C_{trap,0}$	2.0 x 10^{23} m^{-3}	[74]
Φ_{trap}	1.2 eV	[20]
$\hbar\omega_0$	4.0 eV	[67]
m_e^*	0.5m$_e$	[76]
$N_{e,metal}$	8.5 x 10^{28} m^{-3}	[68]
ε_∞	2	[73]
κ	2.5	Reported by GF

Two parameters that vary between different wafers, test structures, or experimental conditions are the minimum dielectric spacing (s), and the substrate temperature (T). Their values are summarized in Table 3.2 for each data set. The nominal dielectric spacing was used for the first two sets of data from the literature due

to limited information. However, the worst case dielectric spacing value was calculated for the experimental data obtained from GLOBALFOUNDRIES. This value is more appropriate to use because the processing can lead to variations in the dielectric thickness, and the sample is most likely to fail where the thickness is the smallest. The worst case dielectric spacing value was calculated using a voltage ramp to determine the breakdown voltage (V_{BD}). A breakdown field (E_{BD}) of 7.5 MV/cm was assumed [77], and the dielectric spacing was calculated as $s=V_{BD}/E_{BD}$.

Table 3.2. Low-κ SiCOH dielectric parameters, determined by the experimental conditions.

	Parameters	
Data Set	***s* (nm)**	***T* (°C)**
Chery et al. [47]	45	125
Croes et al. [72]	37	100
GF	20	125

A deliberate effort was made to limit the number of parameters determined directly from the electrical data, to avoid over-fitting the results. Most lifetime models use two fitting parameters, but are also only applied to failure data, while the charge transport model also applies to conduction data. The model relies on three primary parameters (A_{eff}, Φ_B, and ΔH) that are intrinsic properties of the processed, dielectric material stack. The effective area through which electronic conduction flows in the device structure is denoted as A_{eff}. Since the model is currently a one-dimensional formulation, this parameter is essentially a conversion factor to obtain experimental current values from the predicted mobile electron flux. The energy barrier for electron injection is represented as Φ_B. This parameter might not simply be the barrier height between the Fermi surface of the metal and the conduction band of the dielectric. Defect or interface states located near, or at the cathode, can provide lower energy paths into the dielectric [78]. Φ_B and A_{eff} only require early leakage current vs. field data to determine their values.

Finally, ΔH represents the activation energy for defect formation in the dielectric. This parameter has the largest effect on the magnitude of the time-to-failure. Therefore,

ΔH can be viewed as an overall dielectric strength. The ΔH parameter is determined using a single time-to-failure experimental data point. The results of the model can then be compared to the experimental data at any other applied field keeping all the parameters fixed.

Figure 3.2 shows the experimental and predicted current as a function of applied electric field for the data supplied in Chery et al. [47]. The simulation was able to replicate the current trends fairly well assuming the data reported was the early leakage current. Current as a function of time for the high-field GF data is shown in Figure 3.3. The simulation was able to reproduce the early leakage current as a function of the applied field, the decay in leakage current with stress time, and the abrupt increase in current at failure. The simulation was also able to predict the TTF at each data point within a factor of two or three, which is approximately the standard deviation usually found in TTF data points during testing [62]. The results from Figure 3.2 and Figure 3.3 exemplify one of the advantages of the charge transport (CT) model over the industry-used lifetime models. The CT model is able to replicate the entire history of current flow through the dielectric as a function of time and applied field and, overall, the model predicts failure based on current- and field-driven mechanisms. Even though some of the lifetime models are based on current-driven mechanisms, all of these models are primarily curve fits based only on the time-to-failure data as a function of the applied electric field.

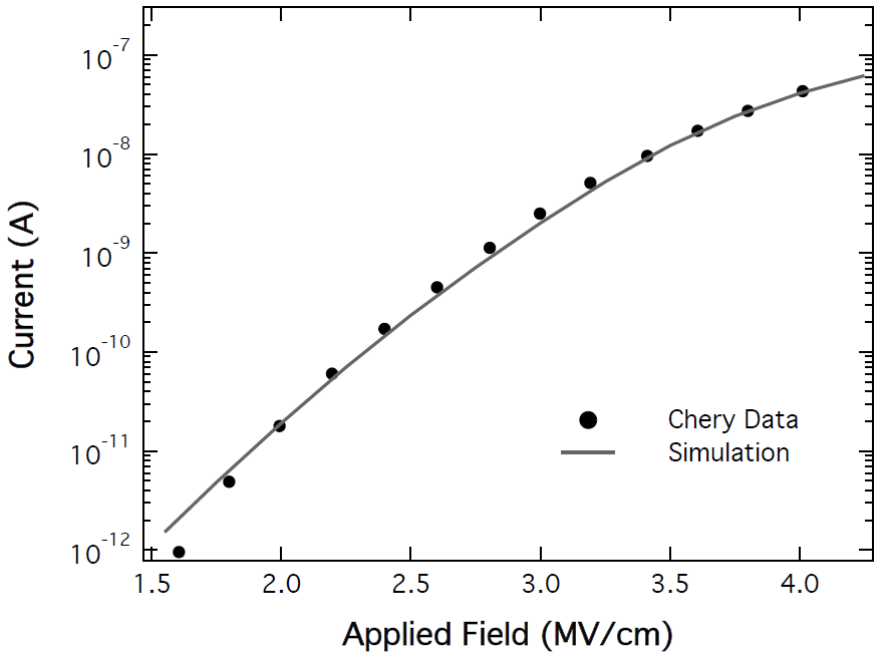

Figure 3.2. Current as a function of Applied Electric Field for low-κ SiCOH experimental data from Chery et al. [47], and the corresponding fit to the data by the charge transport model.

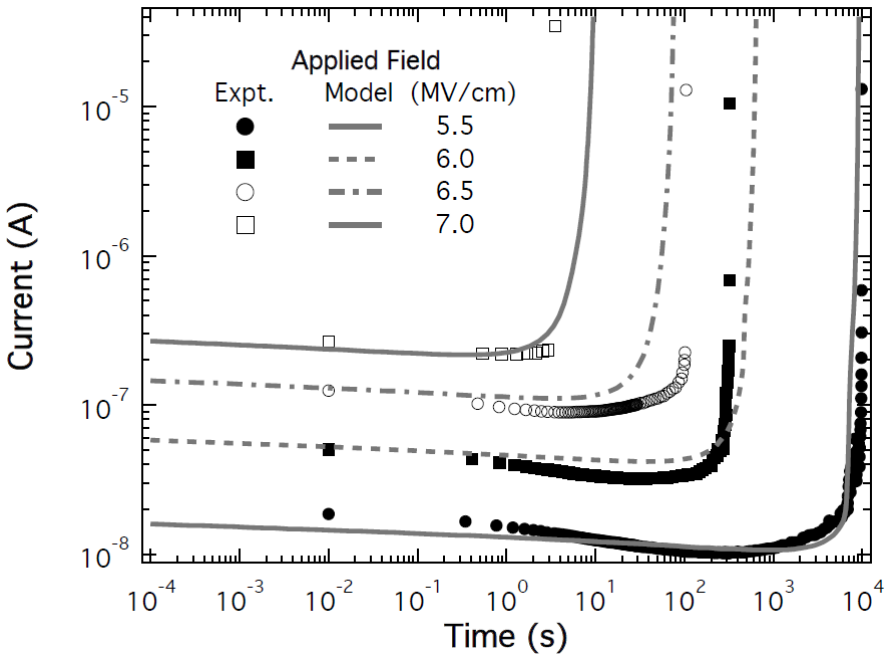

Figure 3.3. Current as a function of time for low-κ SiCOH experimental data obtained from GLOBALFOUNDRIES, and the corresponding fit to the data by the charge transport model.

Figure 3.4 shows the TTF as a function of the applied electric field for the three experimental data sources, as well as the charge transport model's prediction for each case. The results show the CT model is able to accurately predict the TTF within experimental error for all three sources even though the systems used different test structures and slightly different dielectric, barrier, and liner configurations. Figure 3 exemplifies another advantage of the CT model over the lifetime models. The largely empirical models use two (or three, in the case of the LE model) parameters to provide fits to the TTF vs. applied field data. Although the CT model has three unknown parameters, two of these (Φ_B and A_{eff}) are determined based on early leakage current data only. The third parameter, ΔH, is determined based on the TTF of a single voltage data point. Therefore, none of these parameters are adjusted to fit to the slope of the TTF vs. applied field curve, yet the simulation is able to accurately predict this slope for all three sets of experimental data.

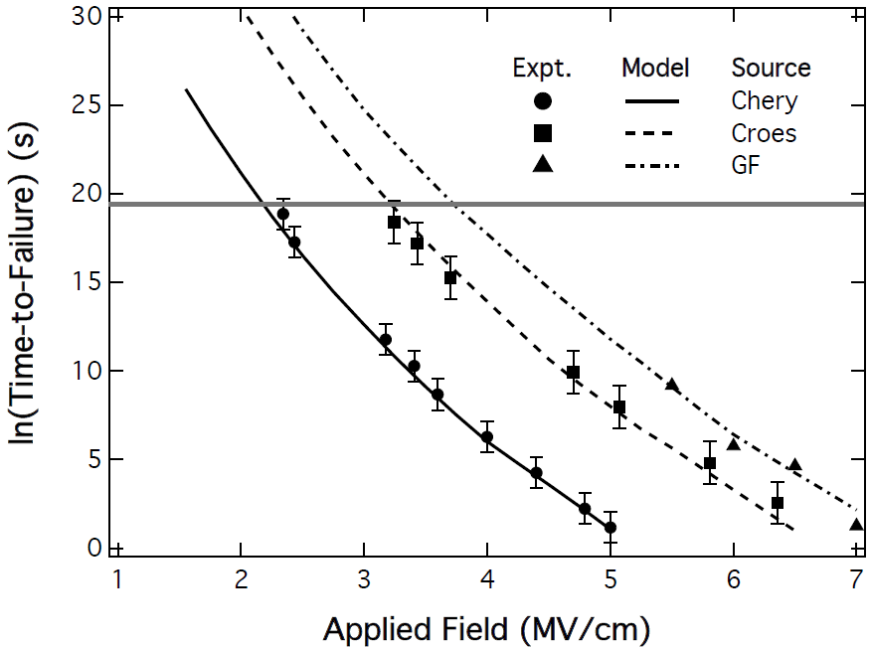

Figure 3.4. Semi-log plot of Time-To-Failure (TTF) versus Applied Electric Field for three sets of low-κ SiCOH experimental data, and the corresponding fits by the charge transport model. The solid gray, horizontal line represents a 10-year lifetime.

The three parameters fitted for each experimental case are shown in Table 3.3. The predicted values for Φ_B in the model correspond well to the 1.1-1.9 eV range of

Cu/low-k barrier heights measured using x-ray photoelectron spectroscopy by King et al. [78]. Although previous investigations using photoemission spectroscopy have measured the optical barrier height into low-k SiCOH dielectrics to be >4 eV [79], [80], the lower electrical barrier height can be attributed to effects of Fermi level pinning due to interface defects [78]. This agrees with the results from Guo, Zheng, et al. [81], who also conducted x-ray photoelectron spectroscopy measurements to show that ion sputtering can lower the low-k dielectric bandgap by up to 2.2 eV due to ion sputtering. Ion sputtering is used to deposit the Ta/TaN barrier and Cu seed layers on the low-k dielectric prior to Cu electroplating to form the metal electrode.

Table 3.3. Low-κ SiCOH dielectric parameters, adjusted based on experimental data.

	Parameters		
Data Set	A_{eff} **(m^2)**	Φ_B **(eV)**	ΔH **(eV)**
Chery et al. [47]	6.0×10^{-18}	1.58	2.43
Croes et al. [72]	2.0×10^{-20}	1.65	2.57
GF	2.5×10^{-18}	1.78	2.74

A_{eff} should be proportional to both the total area of the test structure and the fraction of the structure through which conduction occurs. A_{eff} is on the order of 10^{-18} to 10^{-20} m^2 in the simulations, and electron traps in SiO_2 oxide dielectrics have been found to have capture cross sections in the range of 10^{-18} m^2 to 10^{-23} m^2 [82], [83]. This area increases with increasing hydrogen concentration [82]. Large hydrogen concentrations are characteristic of low-k dielectrics because of the material's composition and its ability to adsorb water during processing. Comparisons between these experimentally measured, capture cross sections and A_{eff} could support the theory of one or multiple percolation paths through the dielectric during stress. However, the meaning of this parameter is still relatively unknown, and could be better understood by developing the model into two- or three-dimensions.

Finally, ΔH is the activation energy for defect formation, and is comparable to the calculated activation energy of 2.3 eV for trap creation by hot electrons in SiO_2 oxides [82]. This energy might be representative of the bond energies being broken in

the dielectric. Si-Si bonds, which are derived from oxygen vacancies, have bond energies of 2.25 eV, while Si-H bonds, hypothesized to be broken in the power law model, have bond energies of 2.5 eV to 3 eV [42]. A third advantage of the CT model over the lifetime models becomes evident; the parameters used in the CT model are consistent with theoretical or experimental values for dielectric materials. Although some of the lifetime models claim to have a theoretical basis for their fitting parameters, these parameters are still primarily data fits and cannot be correlated to material compositions or processing conditions with any degree of confidence.

Figure 3.5 compares the simulation results of the CT model with lifetime models fitted to the experimental data supplied in Chery et al. [47] and Croes et al. [72]. The figures are zoomed in to the low fields because all the models give similar predictions at high fields, as evidenced by the inset in Figure 3.5A. In Figure 3.5A, the low-field predictions by the charge transport model most closely follow the $E^{1/2}$ model, while the power-law model and lucky electron model have lifetime predictions that are more optimistic. The opposite is true for Figure 3.5B, in which the simulation's predictions most closely resemble the power-law model and lucky electron model, while the $E^{1/2}$ model provides a more conservative time-to-failure extrapolation. Thus, the current model can reproduce features associated with a number of the algebraic models currently used in the field despite the fact that it provides a common framework for breakdown independent of testing configuration.

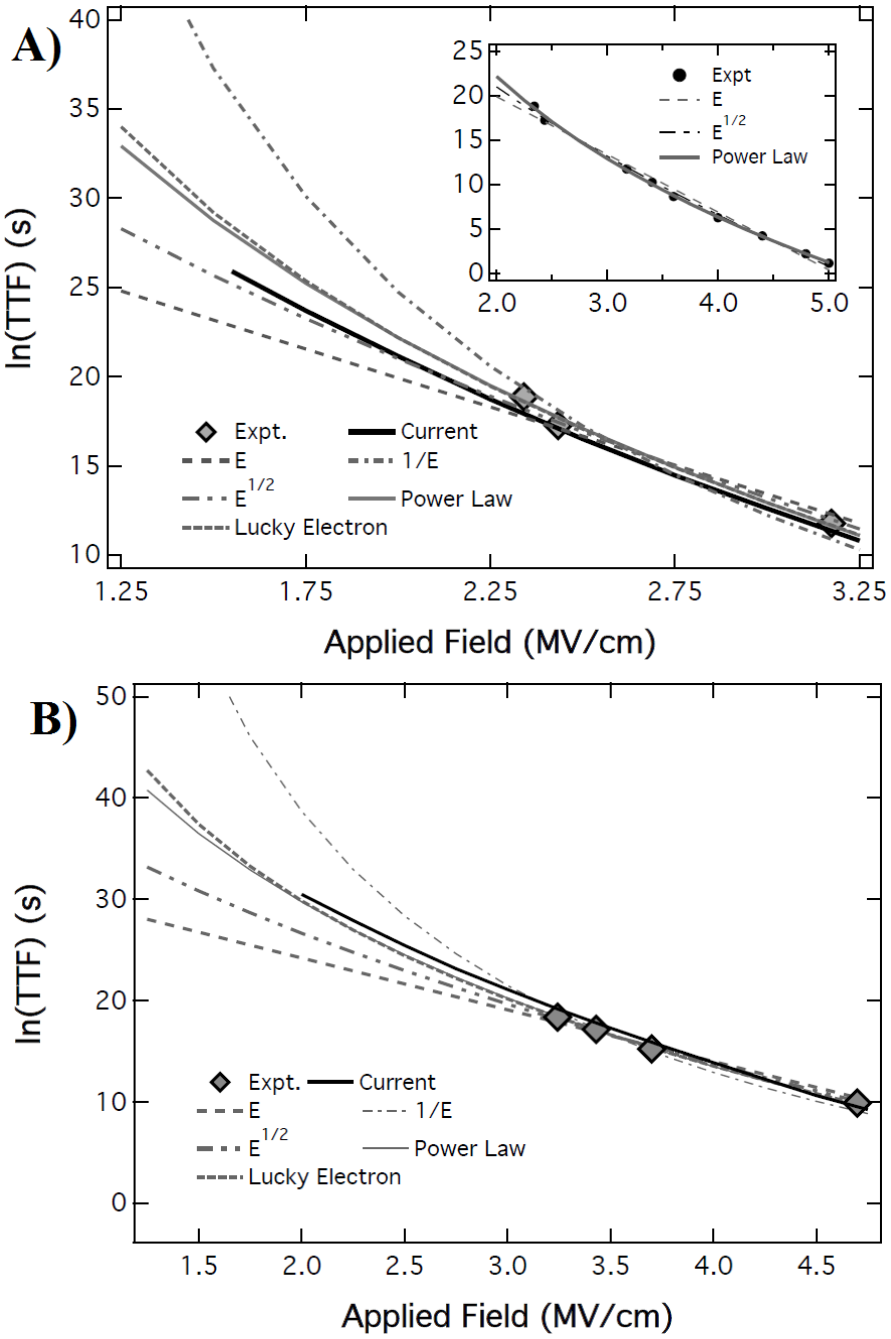

Figure 3.5. Comparisons between the charge transport model (labeled as "current") and various empirical models fitted to experimental data for (A) the Chery results and (B) the Croes results. The inset in (A) shows the convergence of predictions at high fields.

Chery et al. [47] and Croes et al. [72] found that the power law model and lucky electron model were most consistent with their experimental results. This is true for the

findings from other recent low-field tests as well [62], [84], [85]. However, the CT simulation results indicate that the lucky electron model and power law model are too optimistic for some test structures. In addition, the $E^{1/2}$ model is too conservative for other test structures, although using this model is safer than over-predicting TTF. The mechanism of dielectric breakdown is likely too complex a process to represent using a single, lifetime model. The charge transport model, however, incorporates a comprehensive breakdown mechanism, driven by the field as well as the current within a framework that can be easily extended to multiple dimensions, multiple materials, and multiple forms of defect generated in the solid. This model could therefore be used as an aid to tie the materials, processing conditions, test structure, and experimental set-up to the lifetime model fittings, providing valuable insight for both current and future technology nodes in order to improve reliability assessment.

3.4.2 High-κ SiN

Silicon nitride has been employed in a wide range of engineering applications for more than 50 years. Due to its hardness and thermal stability, the ceramics industry has integrated this material for use as bearings [86], in engines and jets as a structural material [86], [87], and for high-speed metal cutting [88]. Silicon nitride also has strong insulating properties, such as a low leakage current and high breakdown field, making the material useful in the electronics industry. Silicon nitride-based materials, typically in the amorphous phase and containing hydrogen (α-SiN:H) and sometimes carbon (α-SiCN:H), have been used as an insulator and/or passivation layer in radio frequency micro-electro-mechanical systems [89], thin-film transistors [90], memory devices [91]–[93], and solar cells [94]. It has also generally been used as an etch stop layer in integrated circuits [95].

Therefore, an understanding of the electronic properties and the overall reliability of α-SiN:H is necessary for continued implementation into future electronic devices. Early studies using electron spin resonance (ESR) identified silicon dangling bonds as the major defect states in α-SiN:H, causing hopping conduction and observed memory behavior [96]–[98]. Mutch *et al.* [32] employed ESR and electrically detected magnetic resonance (EDMR) techniques to directly tie the Si dangling bond in silicon nitride-

based etch stop layers to electron conduction through the dielectric and provide insight into the material's reliability trends. Scarpulla *et al.* [69] and Allers [43] determined that the dominant conduction mechanism through capacitor structures with silicon nitride dielectrics was Poole-Frenkel, leading to the use of the $E^{1/2}$ model for reliability estimates. However, Cui *et al.* [99] tested SiCN:H and concluded the long-term constant voltage tests followed the *E* model, possibly due to copper ions which accelerated failure. The different field dependences between similar dielectric materials create uncertainty in the use of such models for reliability. Furthermore, as size features continue to shrink in electronic devices, the reliability of these dielectric materials will become increasingly important. However, a single, unifying model has not yet been developed for this diverse set of nitride dielectrics to predict and tie the leakage current to reliability trends based on material parameters.

Silicon nitride-based dielectrics typically follow similar $E^{1/2}$ conduction mechanisms (Schottky Emission or Poole-Frenkel). The charge transport model replicates these conduction mechanisms, while neglecting tunneling mechanisms, such as Fowler-Nordheim (FN) tunneling. Voltage ramp data was fitted to the FN tunneling empirical equation (Equation 2.3), and was ruled out as a possible conduction mechanism at high voltages based on the calculated energy barriers. The dominant defect in this SiN material is assumed to be the silicon dangling bond. Therefore, the energy level of this defect measured from the conduction band is 2.2 eV based on a bandgap of 5.3 eV for Si_3N_4 [97]. This is also consistent with recent EDMR studies by Mutch *et al.* [100] that determined the Si dangling bond to be the dominant defect in α-SiN:H and located 3.1 eV above the valence band. The spin density of the Si dangling bond was previously measured by ESR techniques and determined to be $2x10^{23}$ m^{-3} based on a N/Si ratio equal to 1.33 [98]. The effective mass of the electron is defined as $0.5*m_e$ [101], where m_e is the mass of the free electron.

Simulations were run for comparison to experiments conducted by Allers [43]. Allers tested metal-insulator-metal capacitor structures with a stoichiometric silicon nitride (Si_3N_4) dielectric. The silicon nitride dielectric was deposited using PECVD with silane, ammonia and nitrogen as the main reactants, and the capacitors were integrated into AlCu metallization with a Ti/TiN liner system to probe the intrinsic characteristics

of the silicon nitride [43]. A static dielectric constant (κ) of 7.2 and a dielectric constant in the optical limit (ε_∞) of 3.8 were reported, and for the data used in this paper, the samples had a dielectric thickness (s) of 50 nm and were tested at 140 °C [43]. Data was obtained for both voltage ramp and constant-voltage stress tests. Table 3.4 shows the material parameters and test conditions obtained from Allers [43].

Table 3.4. Parameters used in all low-κ SiCOH simulations, based on the given reference.

Parameter	Value	Source
$C_{trap,max}$	1.0 x 10^{29} m^{-3}	Calculated
$C_{trap,0}$	2.0 x 10^{23} m^{-3}	[98]
Φ_{trap}	2.2 eV	[97]
$\hbar\omega_0$	4.0 eV	[67]
m_e^*	$0.5m_e$	[101]
$N_{e,metal}$	8.5 x 10^{28} m^{-3}	[68]
s	50 nm	[43]
T	140 °C	[43]
ε_∞	3.8	[43]
κ	7.2	[43]

The experimental data obtained from [43] include a voltage ramp test with a ramp rate (R) equal to 1 V/s and time-dependent dielectric breakdown (TDDB) tests at several voltages. Using the charge transport model, either test can be replicated by setting the appropriate boundary condition at the anode ($V_{app}=R*t$ for voltage ramp or V_{app}=constant for TDDB). First, the voltage ramp test was used to determine the remaining unknown parameters, shown in Figure 3.6. Two different simulations were run for comparison: P_{eff} as adjustable (3-parameter simulation) and P_{eff} fixed to 10^{-8} (2-parameter simulation). The 3-parameter simulation calculated Φ_B based on the J-V slope at high voltages (pre-breakdown) while P_{eff} was used to match the magnitude of the current density. In the 2-parameter simulation, the J-V slope is independent of the fitting, and Φ_B was used to match the current density magnitude. The low-voltage J-V slope is fixed by the optical limit dielectric constant (ε_∞). In each simulation, ΔH was determined

by the breakdown voltage (V_{BD}), which was defined as the last experimental data point in the voltage ramp (V_{BD}=50.1 V, J=0.5 A/cm^2).

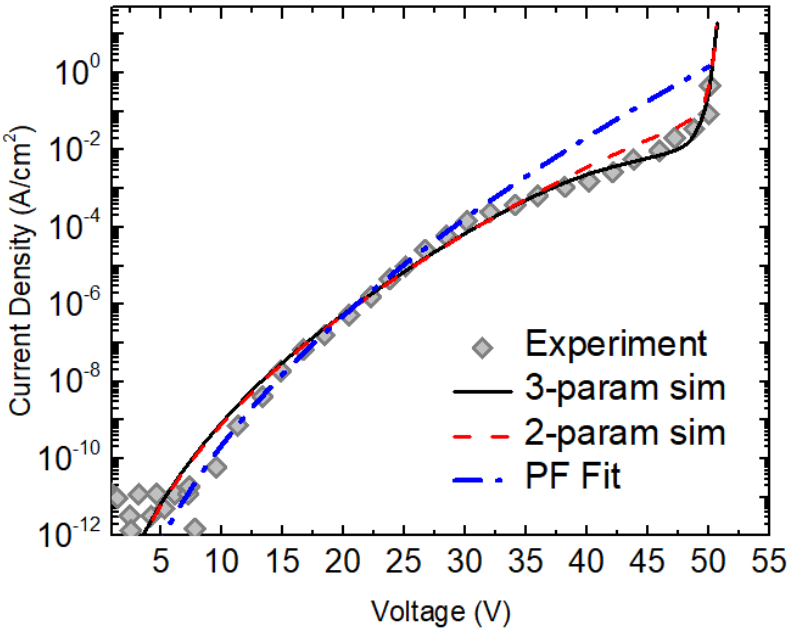

Figure 3.6. Voltage ramp results with experimental data (diamonds) obtained from [43]. The charge transport model results using 3 parameters (black solid line) or 2 parameters (red dash line) predict the high-voltage leakage current while the Poole-Frenkel empirical fit cannot (blue dotted line).

A comparison of the simulations' fits to the *J-V* data was quantified by calculating the adjusted coefficient of determination (R^2-*adj*), given as

$$R_{adj}^2 = 1 - (1 - R^2)\left(\frac{n-1}{n-p-1}\right) \tag{2.17}$$

where R^2 is the coefficient of determination, n is the number of experimental data points, and p is the number of parameters. R^2 was calculated using regression analysis and *ln(J)* as the dependent variable such that all data points were equally weighted. Table 3.5 shows the R^2-*adj* values for the voltage ramp test, divided into low-voltage (10-30 V) and high-voltage (30-50 V) ranges. Both simulations predict a similar current density at low voltages, but the 3-parameter simulation predicts the high-voltage current density better than the 2-parameter simulation. Also shown in Figure 3.6 is a fit to the data using the empirical expression for Poole-Frenkel conduction. Although one can argue the PF equation provides a better fit to the data at low voltages, the charge transport model fits

the high-voltage data dramatically better. In addition, the CT model is able to predict the evolution of the current all the way through the breakdown regime, which is important for reliability purposes.

Table 3.5. Adjusted coefficient of determination (R^2-*adj.*) values for low- and high-voltage *J-V* data from voltage ramp and time-to-failure data for constant voltage stress.

	R^2-*adj.* Values	
Simulation	***J-V* (10-30 V)**	***J-V* (30-50 V)**
3-parameter	0.960	0.927
2-parameter	0.969	0.793

Next, the simulations were run for comparison to the experimental TDDB results. All the parameters were already determined from the voltage ramp data; the only required alteration to the simulations was to set the boundary condition for the voltage at the anode to a constant value. Figure 3.7 shows the experimental and simulation TDDB results. The 3-parameter simulation matches very well with the test data, despite not setting any parameters based on the TDDB experimental results. This is a promising result; the CT model is able to predict the reliability of a dielectric material over several orders of magnitude in time (90 seconds to >1 month) based only on data from a single voltage ramp, requiring less than one minute to test. However, the 2-parameter simulation over-predicts every failure time by a factor of ~2. The 2-parameter simulation is able to fit the TDDB data if ΔH is lowered slightly from 2.73 eV to 2.71 eV (not shown), but it cannot predict the breakdown for the voltage ramp and TDDB tests using the same parameters like the 3-parameter simulation is able to do. The defect concentration was measured throughout the simulations, and the critical density required to cause the abrupt increase in current at failure was determined to be approximately 6×10^{25} traps/m^3 for the voltage ramp simulation and the constant-voltage simulations at various applied voltages. Degrave *et al.* [102] calculated the critical defect density for thin (< 5 nm) SiO_2 gate oxides to be a constant value of 1.3×10^{25} traps/m^3. The simulation's measurement is the same order of magnitude as the value calculated by Degraeve, and the higher value found from the CT model can possibly be explained by

the larger thickness (50 nm) of the silicon nitride film, requiring a larger defect density to form a conductive path compared to the thin gate oxide samples.

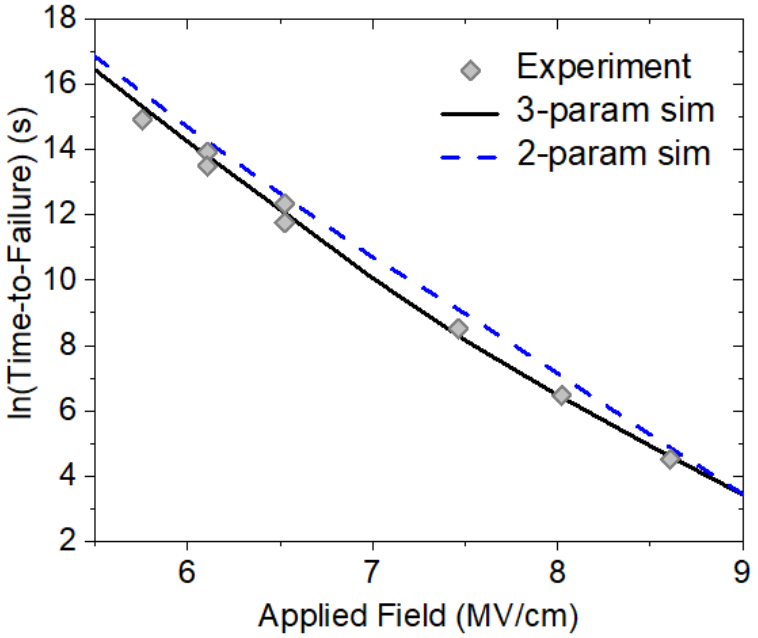

Figure 3.7. Constant-voltage stress failure vs. field results with experimental data (diamonds) obtained from [43]. The 3-parameter simulation (black solid line) show excellent agreement with the experimental data, while the 2-parameter simulation over-predicts the failure times.

An analysis of the adjustable parameters, summarized in Table 3.6, can provide useful information about the model as well as the silicon nitride dielectric. In the 3-parameter simulation, P_{eff} is 20 times smaller than the previously reported value of 10^{-8} [69]. The difference could be due to variations in the materials between [43] and [69], or the assumption made in [69] that the defect density is uniform through the dielectric. Φ_B in these simulations is the energy barrier at the TiN/Si_3N_4 interface and was determined to be 1.53 eV for the 3-parameter simulation and 1.64 for the 2-parameter simulation. This matches closely to the 1.58 eV energy barrier previously estimated for comb-comb SiCOH test structures [103], for which the lowest barrier for conduction is believed to occur at the interface between the metal barrier and etch stop layer (TaN/SiCN:H) [32]. This barrier has been measured to range from 1.45 eV to 2.15 eV, but for higher-nitrogen materials is usually closer to 1.9 eV [104]. The final adjustable parameter (ΔH)

ranged from 2.71 eV to 2.75 eV in the simulations. This parameter represents the weak bonds in the dielectric which are broken under stress conditions. This parameter is similar to the values previously estimated for SiCOH dielectrics (2.43eV to 2.74 eV) [103] and matches the estimated strength of an Si-H bond (2.5 eV to 3.0 eV) [42]. Although Allers [43] prepared Si_3N_4 dielectric capacitors, two of the main reactants were silane (SiH_4) and ammonia (NH_3), which are expected to cause Si-H and N-H bonds to form [95], [98]. N-H bonds have a high bond energy of 4.05 eV [98] and therefore, are expected to break at a much slower rate than Si-H bonds.

Table 3.6. Parameters adjusted based on voltage ramp experimental data. The 2-parameter simulation fixe P_{eff} to the theoretical value determined in [69].

Parameter	Description	3-param Sim	2-param Sim
P_{eff}	Trapping Fraction	5.0×10^{-10}	1.0×10^{-8}
Φ_B	Energy Barrier into Dielectric	1.53 eV	1.64 eV
ΔH	Activation Energy for Defect Formation	2.75 eV	2.73 eV

3.4.3 Comparison of Dielectric Materials

A comparison of low-κ SiCOH and high-κ SiN can provide valuable insight into the reliability and breakdown process of these two materials. Figure 3.8 shows the dielectric failure times as a function of electric field for silicon nitride presented in Section 3.4.2 and for the GLOBALFOUNDRIES test for SiCOH presented in 3.4.1. Even though the GF represented the longest failure times out of the three SiCOH data sets, the silicon nitride film is shown to be more reliable. This is despite the fact that the silicon nitride data is from films fabricated over 10 years prior to the SiCOH films. The results are not entirely surprising, however, because silicon nitride is known to be one of the most reliable dielectric materials.

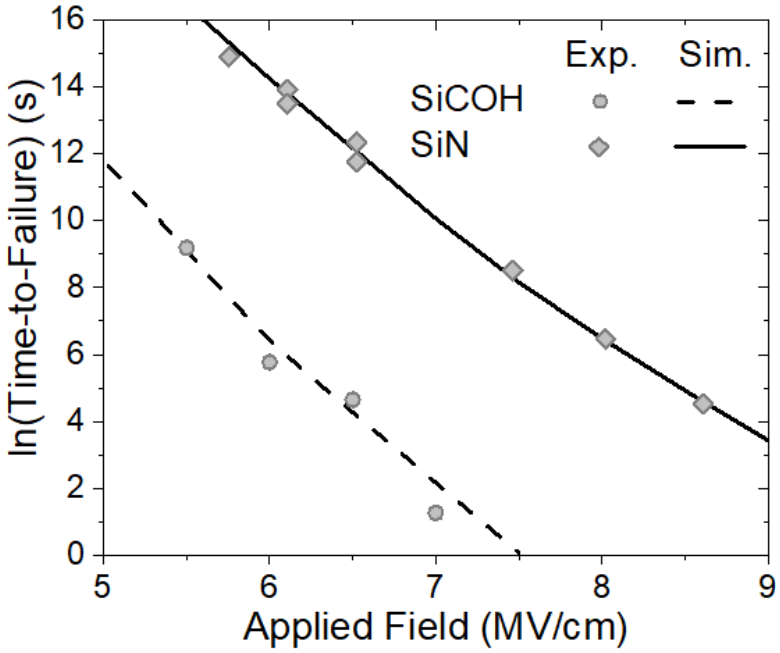

Figure 3.8. Time-to-failure vs electric field for comparison between low-κ SiCOH and high-κ SiN. The low-κ SiCOH data is from the comb-comb structures tested at GLOBALFOUNDRIES, which yielded the longest fail times out of the SiCOH data set. Silicon nitride is drastically more reliability than SiCOH.

The parameters used in the charge transport model for each material can be compared in order to further understand the cause of silicon nitride's superior reliability as an insulator. Table 3.7 shows the most relevant model parameters for silicon nitride and SiCOH, based on the simulations shown in Figure 3.8. The silicon nitride film is thicker (50 nm vs. 20 nm), but the equations presented in Section 3.2 do not yield any significant thickness dependence, in relation to electric field. The initial defect density ($C_{trap,0}$) is important for reliability, but is the same for the films. Interestingly, silicon nitride was tested at a higher temperature (140 °C vs. 125 °C) and was found to have a lower energy barrier for electron injection (1.53 eV vs. 1.78 eV), both of which would decrease the failure time. The higher temperature increases the number of electrons that are able to overcome the energy barrier and also increases the defect generation rate, while the lower energy barrier increases the electron flux.

Table 3.7. Comparison of model parameters between silicon nitride and SiCOH. Silicon nitride's superior reliability can be attributed to its deeper defect energy level and higher dielectric constant.

Parameter	Low-κ SiCOH	High-κ SiN
$C_{trap,0}$	2.0 x 10^{23} m^{-3}	2.0 x 10^{23} m^{-3}
Φ_{trap}	1.2 eV	2.2 eV
s	20 nm	50 nm
T	125 °C	140 °C
ΔH	2.74 eV	2.75 eV
ε_∞	2.0	3.8
κ	2.5	7.2
Φ_B	1.78 eV	1.53 eV

This leaves only a few parameters that can explain the longer failure times for silicon nitride. First, the dielectric constants (κ and ε_∞) are higher for silicon nitride. The higher dielectric constant decreases the electron conduction by affecting the energy barrier, and also decrease the defect generation rate. Second, the energy level of the defects (Φ_{trap}) is 1 eV deeper for silicon nitride compared to SiCOH. The difference in their trap depth is due to the network structure back-bonded to the silicon atom [74] and the energy level of the conduction band between Si_3N_4 and SiCOH [32]. The lower energy level decreases the probability of electrons to be able to tunnel trap-to-trap. Thus, a higher density of defects is required for silicon nitride before failure occurs, increasing its reliability.

One additional parameter that is interesting to compare between these two materials is ΔH. This parameter is essentially identical between SiCOH (2.74 eV) and SiN (2.75 eV). The defect generation process is believed to be due to the breaking of dielectric bonds, and this value indicates that bond being broken is Si-H, which has a bond energy between 2.5 eV and 3.0 eV [42]. Several reliability models propose that Si-H bonds are broken under stress, including the power law model [42] and lucky electron model [46]. The results for the charge transport model support this theory, and find that Si-H is the weak link for two different types of silicon-based dielectrics: SiCOH and

SiN. As discussed in the previous section, most silicon nitride films have some amount of hydrogen due to the deposition process. Si-H bonds being broken under stress, resulting in silicon dangling bonds, will be an important assumption for the model presented in Chapter 4.

3.4.4 Variable Voltage Ramp

A voltage ramp test has been shown to provide useful information about the dielectric, including the type of conduction mechanism, material parameters such as the energy barrier for electron injection, and the overall dielectric strength of the material. These tests are typically fast to run (on the order of minutes), enabling immediate feedback to the engineers about the dielectric reliability. Voltage ramp tests have also been proposed as a method to predict lifetime at operating conditions, in lieu of CVS tests which are more time-consuming. Several studies have investigated failure of gate dielectrics as a function of the voltage ramp rate, finding the breakdown voltage decreases as the ramp rate decreases [40], [105], [106]. These studies offered various explanations for this behavior, including thermal degradation [105] and hole trapping near the cathode [40], [106]. However, there is no general consensus to explain this trend.

This testing method was later applied to SiCOH dielectrics in order to investigate the effects of extrinsic failure due to metal ion migration [30]. Intrinsic (electronic) failure can be differentiated from extrinsic (metal ion migration) failure in two ways. The selection of the metal electrode can dictate the type of failure that occurs. Inert electrodes, such as gold, will not react with the dielectric interface, while reactive electrodes, such as copper, will be oxidized and form ions [30]. For a sample with a reactive electrode, the ramp rate can also affect the failure mode. Intrinsic failure occurs at fast ramp rates, while extrinsic failure occurs at slow ramp rates when the failure times are longer, allowing copper ions to migrate through the dielectric [30].

To replicate these experiments, samples were obtained from Intel on silicon substrates. The silicon was heavily doped in order to imitate a metallic-like electrode for electron injection. 200 nm SiCOH dielectric was grown on the silicon substrate, with a dielectric constant of 3.0. Some samples also contained 25 nm SiCNH layer on top of the SiCOH. The SiCOH dielectric is porous (~7%) and has oxygen to react with the metal

electrode at its interface, but the SiCNH layer is more dense and acts as a type of barrier for metal migration. Metal electrodes were deposited on both the back-side silicon and front-side dielectric using e-beam deposition. The top electrode was either copper, capped with titanium, in order to test a reactive electrode, or gold in order to test an inert electrode. Figure 3.9 shows a side-view schematic of the planar test structures. These test structures are not passivated, leaving them susceptible to moisture ingress and other contamination into the dielectric from the sides of the structure. In order to combat this, tests were run at 175 °C in a nitrogen atmosphere to purge moisture from the samples. Samples were annealed in this environment for 30 minutes prior to testing. A Keithley® 6517B Electrometer was used to supply voltage and measure current for the voltage ramp tests. A positive voltage was applied to the top electrode (Cu/Ti or Au), and the bottom electrode (Al/Si) was grounded. This test set up allows for metal ions from the top electrode to migrate into the SiCNH and/or SiCOH dielectrics. Ramp rates were varied between 0.005 V/s and 20 V/s.

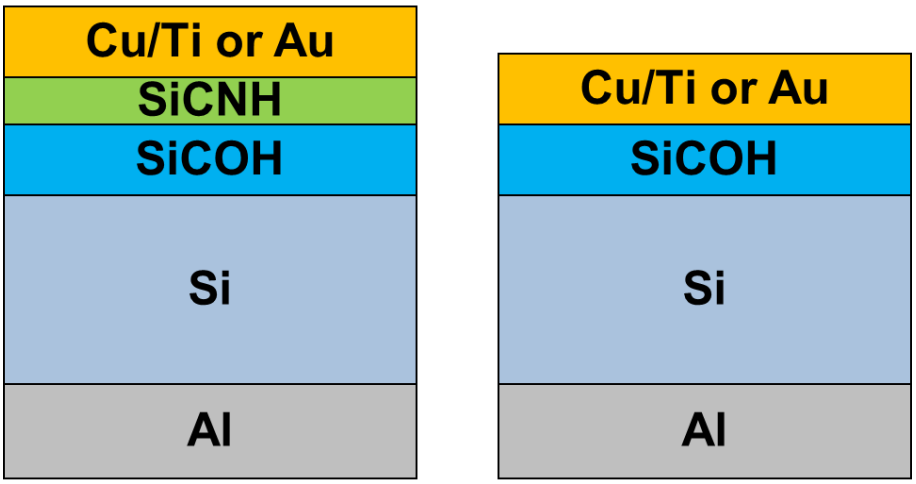

Figure 3.9. Metal-insulator-metal planar test structures used for variable voltage ramp testing. The top electrode was either copper (reactive) or gold (inert). Some samples also comprised of a capping SiCNH layer to block copper ion migration into the SiCOH dielectric.

Figure 3.10 shows the dielectric failure time as a function of the ramp rate on a log-log scale for the various structures that were tested. The SiCOH/SiCNH stack has longer fail times relative to the SiCOH structure at common electric field ramp rates,

regardless of the electrode. This is consistent with the studies in Section 3.4.3 that showed silicon nitride dielectrics are more reliable than SiCOH films. The other interesting comparison is between the samples' *ln(TTF)/ln(R)* slopes. The theoretical limit for intrinsic failure was calculated to be -1, while the best experimental results were -0.94 for inert electrodes [13], [30]. This is consistent with the slopes from Figure 3.10 and shown in Table 3.8. The gold electrode yields a slope equal to -0.94, while the combination of the SiCOH/SiCNH stack with a copper electrode yields a slope equal to -0.95. The addition of the SiCNH capping layer prevents the copper ion migration, as this cap is denser and does not oxidize the copper metals. However, the slope for the SiCOH dielectric without capping layer and with a copper electrode was equal to -0.92. This indicates copper ions are able to enter and move through the SiCOH dielectric, resulting in lower failure times at the lower ramp rates. Similar tests on SiCOH films with a higher porosity (25%) yielded a slope equal to -0.85 due to increased copper solubility and diffusivity into and through the SiCOH dielectric film [30].

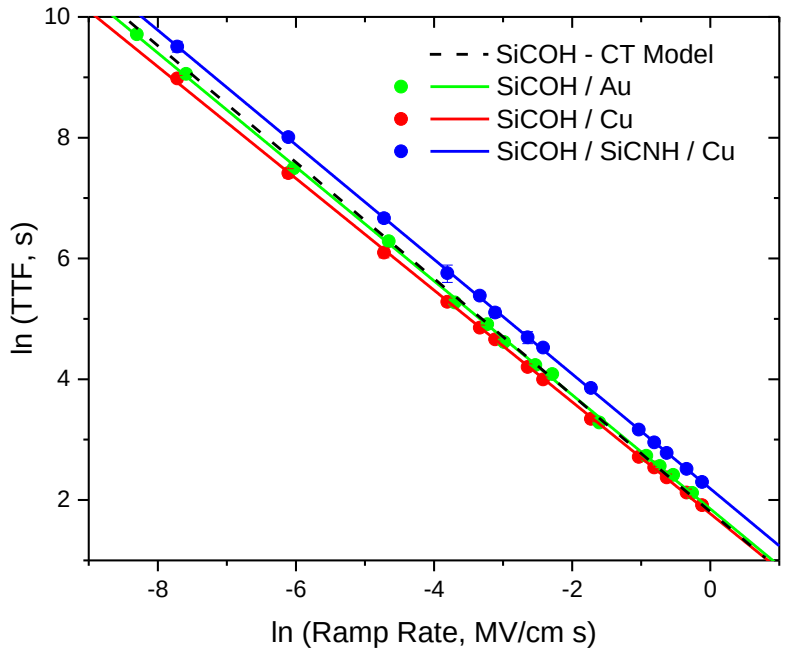

Figure 3.10. Dielectric failure as a function of the electric field ramp rate on a log-log scale for test structures with various dielectric stacks and electrode materials. Gold acts as an inert electrode, while copper acts as a reactive electrode and can migrate into the dielectric under bias or temperature stress.

Table 3.8. Calculated power law exponent for failure as a function of ramp rate. Copper ions migrate into a porous SiCOH dielectric under stress, reducing the exponent from the theoretical limit of -1.

	Dielectric	Electrode	n
Simulation	SiCOH		-0.96
Experiment	SiCOH	Au	-0.94
	SiCOH	Cu	-0.92
	SiCOH/SiCNH	Cu	-0.95

The reduction of the slope due to metal ion migration is well understood. However, even inert electrodes exhibit a reduced slope compared to the theoretical limit of -1. Previous explanations for this trend (thermal degradation and hole trapping) are insufficient. The charge transport model was used to simulate these experiments. The model replicates intrinsic failure, so it can be readily applied for comparison to the samples with the gold electrode. For the simulations, a dielectric constant $\kappa=3$ was used with a dielectric thickness of 200 nm and temperature of 175 °C to match the experimental set-up. The remaining parameters were kept the same as those used in the GLOBALFOUNDRIES simulations from Section 3.4.1, except ΔH which was determined from the dielectric failure at the fastest ramp rate. The simulation results are included in Figure 3.10. The simulations match very closely to the experimental SiCOH data with a gold electrode. The model predicts a slope equal to -0.96, agreeing well with the SiCOH/Au and SiCOH/SiCNH/Cu samples showing intrinsic breakdown. This result indicates that the theoretical slope of -1 is not attainable in practice because the breakdown voltage decreases as the ramp rate decreases. This can be explained through the defect generation rate in the model equations. Slower ramp rates subject the dielectric to electrical stresses for longer periods of time, enabling more defects to generate at each voltage step. The dielectric failure is driven by a critical defect density rather than a critical electrical field. Thus, the breakdown voltage (and overall dielectric strength) is dependent on the ramp rate.

3.5 Model Limitations

The charge transport model provides a comprehensive look at the physical mechanism of dielectric breakdown, and is able to replicate a wide variety of electrical data. The model has thus far re-produced leakage current and dielectric failure for both constant voltage stress and ramped voltage stress. However, the model, as it is presented in this chapter, has several limitations, two of which will be described in this section.

First, the model was found to over-predict the temperature dependence for dielectric failure. Integrated comb-comb structures were tested at GLOBALFOUNDRIES with a dielectric constant κ=2.7. The samples were tested at three voltages, and 3 temperatures for each voltage. Simulations were also run at the same conditions as the experiments, and using the same method to calculate the activation energy for dielectric failure. Figure 3.11 shows the *TTF* activation energy for the experiments and simulations. The experimental data show E_{act} increases as the electric field decreases, consistent with previous findings [49]–[52]. The charge transport model also predicts this same trend, but the model grossly over-estimates the temperature dependence for the failure by greater than 1 eV.

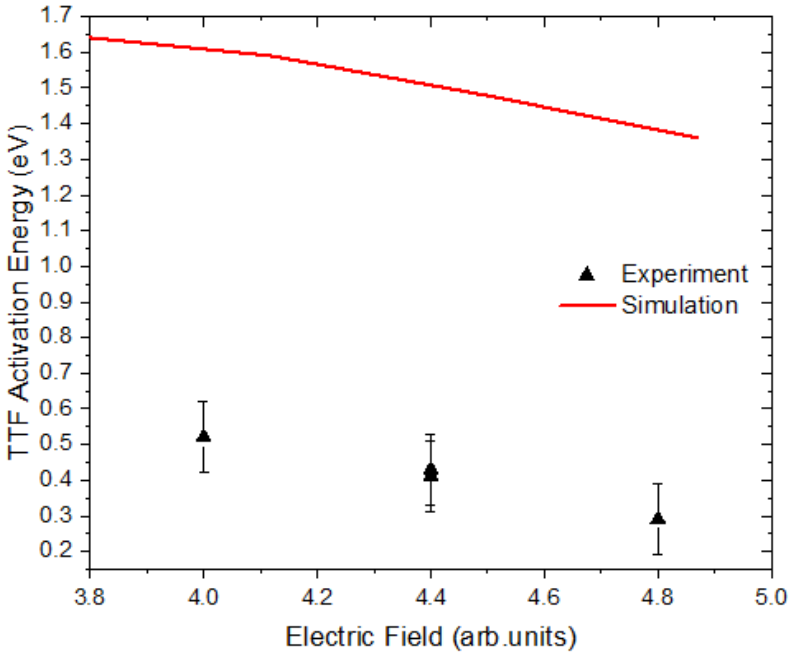

Figure 3.11. Activation energy for dielectric failure (E_{act}) as a function of electric field. Both experimental data and simulations predict the activation energy increases as the electric field decreases, but the simulation over-predicts the activation energy by greater than 1 eV.

There are several temperature dependent variables and equations in the charge transport model, but overall, two equations dominate the temperature dependence for failure. The first is the injection of electrons into the dielectric by overcoming an energy barrier (Equations 2.11 and 2.11a). There is an exponential dependence with the substrate temperature due to the energy barrier, which electrons must overcome to enter the dielectric. Several studies have pointed to the electron conduction as the root cause for the voltage-dependent activation energy for dielectric failure [51], [52]. The second contributing factor in the equations to the failure's temperature dependence is the defect generation equation (Equation 2.8). Defect generation has an exponential dependence to the electron temperature (T_e), which is elevated above the lattice temperature (T). At first glance, it appears there should not be any substrate temperature dependence to the failure due to the elevated T_e which is a function of the electric field. However, T_e is also a function of the defect density, such that the electron temperature decays as defects are generated. Figure 3.12 shows the simulation results of the electron temperature as a

function of stress time at various electric fields. The stress time is normalized to the failure time. During the initial stress, the electron temperature is a function of the electric field. However, as defects are generated, T_e decays towards the substrate temperature (labeled as the black, dotted line), reaching the substrate temperature at the failure point. The decaying temperature provides an increased activation energy for failure, resulting in the model's over-prediction compared to the experimental data. This provides evidence that the equation for T_e is fundamentally flawed. The electron temperature should be a function of the electric field, and the experimental data suggests it should not contribute to the dielectric failure activation energy. In Chapter 4, the theory for the electron temperature will be re-visited, and the equation will be revised based on an improved understanding of the electron's interaction with the dielectric matrix.

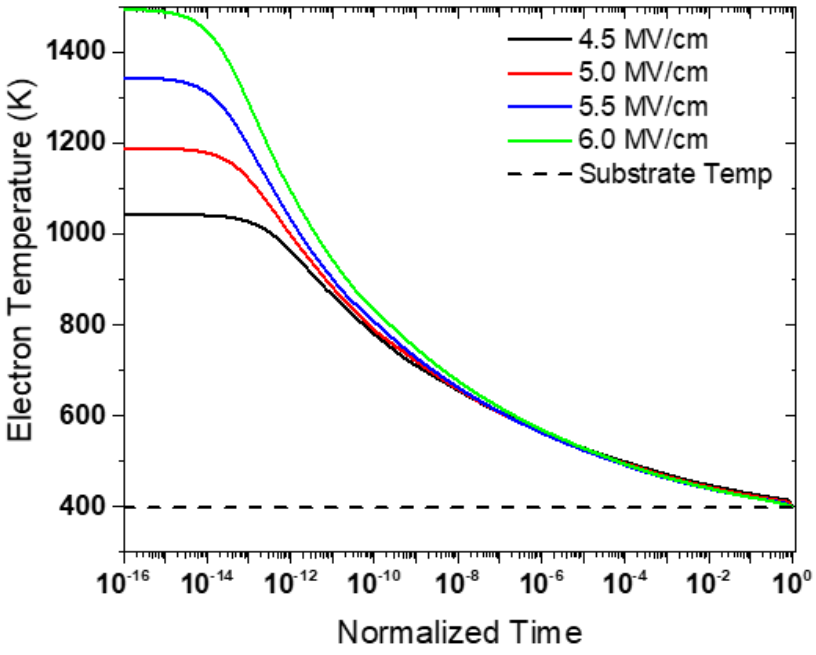

Figure 3.12. Electron temperature simulations as a function of time at various electric fields. The time is normalized to the time-to-failure. The electron temperature decays towards the substrate temperature as defects are generated, removing the field dependence in the equation and instead causing a temperature dependence in the dielectric failure.

The second model limitation is related to the dielectric thickness. The charge transport model incorporates the dielectric thickness into its boundary conditions, but

this parameter is not included in any other variables or equations. Therefore, the charge transport model claims there is no thickness dependence to the dielectric failure, as related to the electric field (essentially, two samples with different thicknesses will fail at the same time if stressed at the same electric field). Figure 3.13 shows the simulation results for a SiCOH dielectric material at three thicknesses (5 nm, 10 nm, and 20 nm). The failure times are similar between the various thicknesses, with the 20 nm sample showing shorter failure times by a factor of ~2. The shorter failure time is attributed to differences in the local electric fields in the dielectric. Based on Poisson's equation, the electric field is non-constant across the dielectric due to the build-up of positive or negative charge.

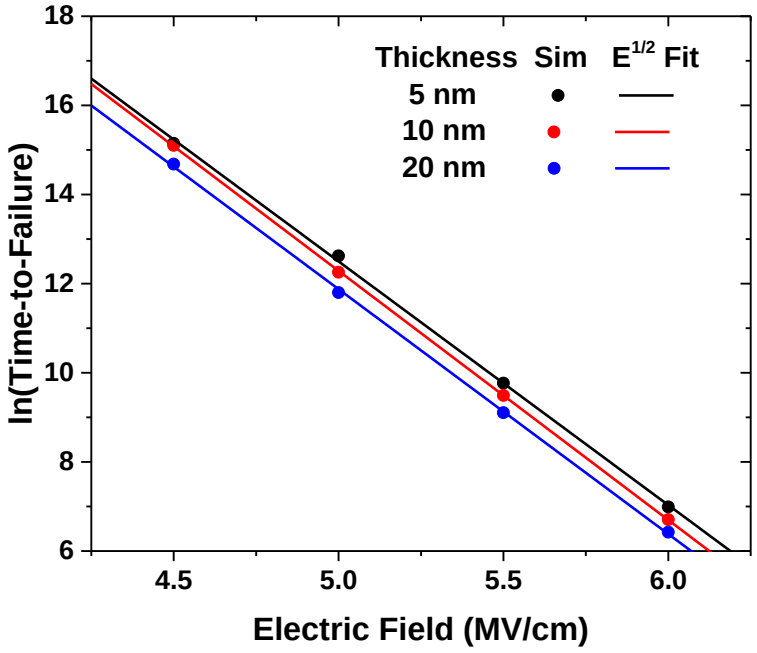

Figure 3.13. Simulations to predict dielectric failure as a function of thickness. A small boost in overall time-to-failure is observed as the dielectric thickness decreases, but there is no change in the failure versus electric field slope as predicted by the $E^{1/2}$ model.

The simulations were fitted to the $E^{1/2}$ model in order to assess if there is any change in the slope for dielectric failure as a function of electric field. The choice of model is arbitrary in this evaluation; the goal is only to compare the slope values. Table 3.9 shows the fitting parameter values from the $E^{1/2}$ model, as well as the lifetime projection near

the operating conditions equal to 1 MV/cm. The failure vs field slope (γ) varies less than 2% between the three samples of varying thickness, and the lifetime projections are all similar as well.

Table 3.9. Fitting parameter values using the $E^{1/2}$ model from simulation results for various dielectric thicknesses. The model parameters and lifetime projection near operating conditions equal to 1 MV/cm are similar between 5 nm, 10 nm, and 20 nm samples, indicating practically zero thickness dependence for dielectric failure.

Thickness	A	γ	Lifetime @ 1 MV/cm (yrs)
5 nm	2.0×10^{17}	5.5	2.7×10^{7}
10 nm	3.0×10^{17}	5.6	3.5×10^{7}
20 nm	1.2×10^{17}	5.5	1.6×10^{7}

There is a lot of ongoing debate between reliability engineers for TDDB centered on the thickness dependence for dielectric failure. Several studies on planar SiCOH dielectrics have shown the dielectric strength of an insulator will increase as the dielectric thickness decreases [107], [108]. A recent report has provided a theoretical explanation, generic to all dielectric materials, for this trend [109]. McPherson showed the dipole moments, which enhance the electric field and weaken bonds, are a function of the dielectric thickness. As the thickness decreases, the dipole moments are increasingly constrained by the surface dipoles, which do not enhance the field as much as the bulk dipoles [109]. McPherson's theory agreed well with experimental data. In Chapter 4, this theory will be discussed in more detail, and the equations will be revised to incorporate this thickness dependence into the model.

4. REFINED CHARGE TRANSPORT MODEL

In the last chapter, the charge transport model's limitations were outlined in comparison to existing dielectric failure data. In this chapter, the model's equations are refined to expand its failure prediction capabilities. The equation for the electron temperature is re-defined based on an improved understanding of energy transfer mechanisms within the dielectric. In addition, the defect generation rate is aligned more properly with the thermo-chemical *E* model, which also predicts bond breakage as the mechanism for failure, and has recently been proposed to have a thickness dependence. The equations are also converted into a dimensionless form to explore the transport properties, reaction kinetics, and details of the breakdown process. The new forms of equations are shown to predict dielectric failure as a function of voltage, temperature, and thickness. Finally, the model is used to explore dielectric failure trends for future generation devices.

"All models are wrong, some are useful."

-George Box

4.1 Refined Model Equations

The charge transport model is comprised of a set of nonlinear, time-dependent, partial differential equations, and is developed to predict the intrinsic (or electronic) failure of dielectric materials [110]. The model's basic concepts are as follows: Electrons are injected into the dielectric over an energy barrier, and their conduction is dictated by the existing defects in the dielectric. The conducting electrons gain energy from the electric field and lose energy to collisions with the dielectric matrix. New defects are created

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Portions of this chapter have been submitted to: S. P. Ogden, Y. Xu, K. B. Yeap, T. Shen, T.-M. Lu, and J. L. Plawsky, "Charge transport model to predict dielectric breakdown as a function of voltage, temperature, and thickness," *J. Appl. Phys.*, submitted for publication.

Portions of this chapter appeared in: S. P. Ogden, K. B. Yeap, T. Shen, P. Justison, T.-M. Lu, and J. L. Plawsky, "Method to determine the root cause of low-κ SiCOH dielectric failure distributions," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 119–122, Jan. 2017.

when an electron transfers enough energy to physically break a bond by displacing an atom [46]. As the concentration of defects increases, the probability for electrons to tunnel directly between traps also increases. At a critical defect density, this tunneling mechanism is accelerated and becomes the dominant conduction mechanism. The increasing electron current further accelerates the generation of new defects, causing a positive feedback (or feed-forward) mechanism [106] and resulting in an abrupt increase in current seen at failure. The model can be represented in dimensional or dimensionless form.

4.1.1 Dimensional Form

The potential distribution and the local electric field, $F = -\partial V / \partial x$, are affected by the accumulation of charge in the dielectric, and obey Poisson's Equation:

$$\frac{\partial^2 V}{\partial x^2} = \frac{q}{\kappa \varepsilon_0}\left(C_{trap} - C_{e,mob,total} - C_{e,trapped}\right), \tag{4.1}$$

where q is the fundamental unit of charge, such that $q < 0$, ε_0 is the vacuum permittivity, and κ is the dielectric constant. Overall, the dielectric is nearly neutral, but the buildup of charge affects the local electric field. The accumulation of positive charge enhances the field at the cathode, while a net negative charge reduces the field at the cathode. C_{trap} is the concentration of defects, or traps, in the dielectric. For low-κ SiCOH, as well as other silicon-based dielectrics, these traps are assumed to be silicon dangling bonds. Therefore, they have an associated positive charge and are donor-like in nature [61], [62].

Electrons are defined as either mobile ($C_{e,mob,total}$) or trapped in the dielectric ($C_{e,trapped}$). Their continuity equations are expressed as:

$$\frac{\partial C_{e,mob,total}}{\partial t} + \frac{\partial}{\partial x}\left(J_{e,mob,total}\right) = g_{e,tunnel} - \frac{\partial C_{trap}}{\partial t} \tag{4.2}$$

and

$$\frac{\partial C_{e,trapped}}{\partial t} = \frac{\partial C_{trap}}{\partial t} - g_{e,tunnel}, \tag{4.3}$$

where

$$J_{e,mob,total} = v_e C_{e,mob,total} - D_e \frac{\partial C_{e,mobile}}{\partial x}. \tag{4.2a}$$

There are two types of mobile electrons: $C_{e,mobile}$ refers to thermally excited electrons traveling above the conduction band in the dielectric, and $C_{e,tunnel}$ represents electrons that tunnel directly between adjacent traps, such that $C_{e,mob,total} = C_{e,mobile} + C_{e,tunnel}$. The mobile electron flux through the dielectric is represented as $J_{e,mob,total}$. Both thermally excited electrons and tunneling electrons have drift components in the flux term, but tunneling electrons are not able to diffuse through the dielectric. Trapped electrons are immobile. The electron velocity and diffusion coefficient for the mobile electrons are defined as:

$$v_e = \frac{qF}{|qF|}\left(\sqrt{\frac{|qF\lambda_{trap}|}{m_e^*}} + \sqrt{\frac{8k_bT}{\pi m_e^*}}\right) \tag{4.4}$$

and

$$D_e = \lambda_{trap}\sqrt{\frac{k_bT}{3m_e^*}}, \tag{4.5}$$

where m_e^* is the effective electron mass, k_b is the Boltzmann constant, T is the substrate temperature, and λ_{trap} is the scattering length between defects. The effective mass of the electron is defined as $0.5m_e$ [50], where m_e is the mass of a free electron. The electrons are represented with an average bulk velocity that consists of a field component, as well as a thermal component included for a lower bound. Electrons are accelerated by the electric field, and scattering events will limit their velocity. Electron scattering can occur due to phonons or defects. Phonon scattering can be divided into two types: acoustic and optical. Acoustic scattering is only important at high fields of ~10 MV/cm [8], and thus, will be ignored. Therefore, 10 MV/cm becomes the upper limit for the model equations. Optical phonon scattering is pre-dominantly a forward scattering mechanism [57], [76], and does not need to be considered for velocity. However, optical phonon scattering will be considered later for electron temperature. For defect scattering, electrons can either be trapped or back-scattered in the dielectric. Thus, the electron velocity is related to the distance electrons can travel between defects. The electron velocity is in the opposite direction as the electric field. The diffusion coefficient is obtained assuming that the

scattering time is independent of the relaxation time between events and independent of the field [63].

The scattering length between defects is based on a Debye length [64]:

$$\lambda_{trap} = \left(\frac{\kappa \varepsilon_0 k_b T}{q^2 C_{trap}} \right)^{1/2} . \tag{4.6}$$

The scattering length is inversely proportional to the square root of the trap concentration, and represents the distance beyond which electrons are unaware of other charges, such as defects or trapped electrons. The Debye length is used because the defects have a positive charge.

Electrons are trapped in the dielectric at the same rate that defects are generated, which is to say that every time a defect is created, that defect immediately traps an electron. Electrons trapped in the dielectric can gain mobility by tunneling through the dielectric trap-to-trap. The rate at which tunneling electrons are generated is derived as:

$$g_{e,tunnel} = \frac{\partial}{\partial t} \left[C_{e,trapped} \exp\left(- \frac{4\sqrt{2m_e^*}}{3\hbar |qF|} \phi_{trap,eff} \right) \right], \tag{4.7}$$

where $\hbar$ is the reduced Planck constant. The tunneling electron generation rate is proportional to the concentration of electrons trapped in the dielectric. It is also proportional to the WKB tunneling probability, represented as the exponential function in Equation 4.7. The trapped electrons must overcome an effective energy barrier to escape the trap in which they are confined. This effective energy barrier is defined as:

$$\phi_{trap,eff} = \phi_{trap}^{3/2} - \left(\phi_{trap} - |qF\lambda_{trap}| \right)^{3/2}, \tag{4.7a}$$

where Φ_{trap} = 1.2 eV is the generic barrier height for traps [20]. As the defect concentration increases and thus, the scattering length decreases, the probability for trapped electrons to tunnel through the dielectric increases.

The rate of defect generation is expressed as a second order chemical reaction between the mobile electrons and the dielectric matrix.

$$\frac{\partial C_{trap}}{\partial t} = \eta \left(\frac{\nu_e}{\lambda_{trap}} C_{e,mob,total} \right) \left(\frac{C_{trap,\max} - C_{trap}}{C_{trap,\max}} \right) \exp\left(- \frac{\Delta H_{eff}}{k_b T_e} \right). \tag{4.8}$$

Traps are confined to the matrix, and therefore only have a generation term because their creation is assumed to be irreversible. Electron diffusion is assumed to have a negligible effect on trap creation so that only the electron's drift component is included. A self-limiting reaction mechanism is included based on the maximum number of available trap sites, denoted as $C_{trap,max}$. For a silica-based dielectric, the maximum number of traps is based on the number of fundamental silicon units, such as silica tetrahedra, comprising the dielectric. $C_{trap,max}$ = 1 x 10^{29} m^{-3} is used in this paper. η is a dimensionless fitting parameter used to predict the dielectric failure time. It is at least partially related to the fraction of the dielectric through which conduction, and therefore defect generation, takes place [69], [111]. The enthalpy of activation (ΔH) is the energy required to break a bond, which is weakened by the local electric field:

$$\Delta H_{eff} = \Delta H - q\alpha F_{polar}, \tag{4.8a}$$

where α is the effective molecular dipole moment for the bond which is broken during stress, assumed to be Si-H for silica-based dielectrics [46], [103], [111]. For Si-H, ΔH = 3 eV [42] and α = 7 A° [112]. The dielectric molecules re-arrange under the electric field, creating a dipole moment that enhances the field and is described as:

$$F_{polar} = F\left[1 + L(\kappa - 1)\right], \tag{4.8b}$$

where L is the Lorentz factor, defined by the dielectric thickness [109]. Previously, the Lorentz factor was assumed to be a constant value equal to 1/3 [66], [103]. However, a recent study by McPherson showed L is a function of dielectric thickness [109]. As the thickness increases, the bulk dipoles start to dominate over the surface dipoles, causing the Lorentz factor to increase and the dielectric strength of the material to decrease as the polarized field (F_{polar}) becomes much increasingly larger than the overall electric field (F) [109].

The electron temperature plays an important role in generating defects. As electrons gain energy from the electric field, their temperature increases. If the concentration of electrons is at least 1 x 10^{20} atoms/m^3 (considered the lower limit for the model), the electrons exchange energy with each other faster than they do with the lattice, and the electrons reach an equilibrium temperature greater than the substrate

temperature [113], [114]. In this case, the electrons can be modeled using an effective temperature [115]–[117]:

$$T_e = T + \frac{2qF\lambda_{op}}{3k_b}, \tag{4.8c}$$

where

$$\lambda_{op} = \alpha \tanh\left(\frac{E_p}{2k_bT}\right). \tag{4.8d}$$

The electron temperature is determined based on the energy gained by the electric field versus the energy transferred to the lattice. Defect scattering is assumed to be either an elastic collision (limiting electron velocity) or an inelastic collision (electron becomes trapped). Neither will affect the temperature of the mobile electrons. However, optical phonon scattering has been shown to be the dominant mode of energy transfer to the lattice [57], [113], [118]. Equation (8d) represents the optical phonon scattering length (λ_{op}), which is a function of temperature. An optical-phonon energy (E_p) of 0.070 eV is used [118].

This model can be solved in one dimension with the use of boundary conditions and initial conditions for Poisson's Equation and the continuity equations for mobile electrons, trapped electrons, and traps. The cathode is defined as $x = 0$ and the anode is defined as $x = s$, where s is the minimum dielectric thickness. This thickness is calculated using $s = V_{BD}/E_{BD}$ [27], [29], where E_{BD} is the dielectric strength (0.75 V/nm [29]) and V_{BD} is the average breakdown voltage. The boundary conditions are given as:

$$V(x=0,t) = 0, \tag{4.9}$$

$$V(x=s,t) = V_{app}, \tag{4.10}$$

$$C_{e,mob,total}(x=0,t) = N_{e,metal}\left[\exp\left(-\frac{\phi_{B,eff}}{k_bT}\right)\right], \tag{4.11}$$

where

$$\phi_{B,eff} = \phi_B - \left(\frac{\left|q^3F\right|}{\pi\varepsilon_\infty\varepsilon_0}\right)^{1/2}, \tag{4.11a}$$

and

$$C_{e,mob,total}(x = s,t) = 0, \tag{4.12}$$

where ε_∞ is the dielectric constant in the optical limit. ε_∞ is directly related to the dielectric constant κ, and a value of 2 is used here [73]. The cathode is grounded while a positive potential is applied to the anode, although this boundary condition can be easily altered to apply a negative or variable bias. Electrons are injected into the dielectric at the cathode through a modified Schottky conduction mechanism. The electrons in the metal must overcome an energy barrier, Φ_B, to enter the dielectric. This energy barrier is lowered by the local electric field with a $F^{1/2}$ dependence seen in Schottky emission or Poole-Frenkel conduction. The concentration of electrons at the cathode, $N_{e,metal}$, is assumed to be $8.5\text{x}10^{28}$ m^{-3}, based on one electron per copper atom [68]. The concentration of electrons is set equal to zero at the anode assuming that all the electrons reaching the anode escape the dielectric. This leads to the maximum electron current. The initial conditions are specified as:

$$C_{e,mob,total}(x, t = 0) = 0, \tag{4.13}$$

$$C_{e,trapped}(x, t = 0) = 0, \tag{4.14}$$

and

$$C_{trap}(x, t = 0) = C_{trap,0}. \tag{4.15}$$

Initially, there are no mobile or trapped electrons in the dielectric, but there are defects present, given as $C_{trap,0} = 2\text{x}10^{23}$ m^{-3} [69].

The set of non-linear partial differential equations is solved using COMSOL, a finite-element based modeling software. However, other commercial or home-made software can be used as well. The leakage current through the dielectric is related to the mobile electron flux using:

$$I = qA_{eff} J_{e,mob,total}, \tag{4.16}$$

where A_{eff} is the effective area for electronic conduction. This dimensional form of the equations will be used in this chapter for comparison to experimental data.

4.1.2 Dimensionless Analysis

The equations presented in the previous section are useful to compare to experimental data and extract the unknown parameters. However, a dimensionless form of these equations can provide valuable information about the system's transport properties, reaction kinetics, and overall breakdown process. For simplicity, all variable names from the previous section are unchanged in this section, and the dimensionless variables are defined with a new name.

In order to convert the equations, the independent (x, t) and dependent (V, $C_{e,mob,total}$, $C_{e,trapped}$, C_{trap}) variables first need to be re-defined in dimensionless terms. The length scale is given as:

$$\xi = \frac{x}{s}, \tag{4.17}$$

such that the spatial boundary conditions scale from 0 to 1. The time constant is defined as the Fourier Number:

$$\tau = \frac{tD_{e0}}{s^2}, \tag{4.18}$$

where D_{e0} is the initial diffusion coefficient:

$$D_{e0} = V_T \sqrt{\frac{\kappa\varepsilon_0}{3m_e^* C_{trap,0}}}, \tag{4.18a}$$

and V_T is the thermal energy:

$$V_T = \frac{k_b T}{q}. \tag{4.18b}$$

The diffusion coefficient (D_e) is a function of time, decreasing with increasing defect density. Therefore, an initial diffusion (D_{e0}) is used to define the time constant in order to avoid a non-linear relationship between t and τ.

The dimensionless voltage is given as:

$$\upsilon = \frac{V}{V_{app}}. \tag{4.19}$$

The electron and defect densities are all scaled by the same constant value for simplification purposes. Mobile electrons in the dielectric ($C_{e,mob,total}$) are derived from

the electrons in the copper cathode ($N_{e,metal}$ = 8.5 x 10^{28} atoms/m^3), while trapped electrons ($C_{e,trapped}$) and defects (C_{trap}) are limited by the maximum defect density ($C_{trap,max}$ = 1 x 10^{29} atoms/m^3). Since $N_{e,metal} \approx C_{trap,max}$, all concentration variables are scaled according to $N_{e,metal}$, such that the mobile electron concentration is given as:

$$\theta_{e,mob.total} = \frac{C_{e,mob,total}}{N_{e,metal}} = \frac{C_{e,mobile} + C_{tunnel}}{N_{e,metal}}, \tag{4.20}$$

the trapped electron concentration is represented as:

$$\theta_{e,trapped} = \frac{C_{e,trapped}}{N_{e,metal}}, \tag{4.21}$$

and the defect density is:

$$\theta_{trap} = \frac{C_{trap}}{N_{e,metal}}. \tag{4.22}$$

Next, Poisson's equation and the continuity equations for electrons and defects can be re-arranged into dimensionless form. Poisson's Equation takes the form:

$$\frac{\partial^2 \upsilon}{\partial \xi^2} = Q\theta_{charge}, \tag{4.23}$$

where:

$$Q = \frac{E_B}{E} = \frac{s}{V_{app}} \frac{qsN_{e,metal}}{\kappa \varepsilon_0} \tag{4.23a}$$

and

$$\theta_{charge} = \theta_{trap} - \theta_{e,mob,total} - \theta_{e,trapped}. \tag{4.23b}$$

The non-linearity of the voltage drop through the dielectric depends on the total charge build-up in the dielectric, either positive or negative, and the dimensionless variable Q. Q is the ratio of a type of built-in electric field (E_B) to the nominal electric field. E_B is proportional to the dielectric thickness and inversely proportional to the dielectric constant. Thus, at common nominal E fields, Q increases as the dielectric thickness increases. This provides an explanation for the trend observed in Chapter 3, where the failure time slightly decreased for thicker dielectrics. A higher Q value for thicker dielectrics creates more linearity in the voltage drop, creating a higher local electric field

near the cathode due to a buildup of negative charge. The local electric field is defined as:

$$\psi = -\frac{\partial \upsilon}{\partial \xi} \tag{4.24}$$

The continuity equations for mobile and trapped electrons are defined as:

$$\frac{\partial \theta_{e,mob,total}}{\partial \tau} + \frac{\partial}{\partial \xi}\left(\delta_{e,mob,total}\right) = \chi_{e,tunnel} - \frac{\partial \theta_{trap}}{\partial \tau} \tag{4.25}$$

and

$$\frac{\partial \theta_{e,trapped}}{\partial \tau} = \frac{\partial \theta_{trap}}{\partial \tau} - \chi_{e,tunnel}, \tag{4.26}$$

where

$$\delta_{e,mob,total} = \frac{D_e}{D_{e0}}\left(Pe\,\theta_{e,mob,total} - \frac{\partial \theta_{e,mobile}}{\partial \xi} \right). \tag{4.25a}$$

Pe is the Péclet number, which for mass transport, represents the relevance of convection to diffusion [119]. The Péclet number is given as:

$$Pe = \frac{v_e s}{D_e}. \tag{4.25b}$$

Convection is measured by the electron velocity (v_e), while diffusion is also measured as a speed (D_e/s). A large Péclet number (>>1) indicates convection-dominated transport, while a low *Pe* defines diffusion-dominated transport, which results in an electron concentration gradient through the dielectric [119]. Based on Equations 4.25a and 4.25b, it is expected that the electron flux decreases over time as the electron velocity and diffusion coefficient decay due to the buildup of defects in the dielectric. The dimensionless form for the tunneling electron generation rate is expressed as:

$$\chi_{e,tunnel} = \frac{\partial}{\partial \tau}\left[\theta_{e,trapped} \exp\left(-\frac{4s\sqrt{2m_e^*}}{3\mathrm{h}V_{app}|q\psi|}\phi_{trap,eff} \right) \right] \tag{4.27}$$

and the dimensionless defect generation rate is:

$$\frac{\partial \theta_{trap}}{\partial \tau} = Da\left(\frac{D_e}{D_{e0}} \right)\theta_{e,mob,total}\left(1 - \theta_{trap}\right). \tag{4.28}$$

In its dimensionless form, the defect generation rate is proportional to the Damköhler number, which represents the importance of the reaction relative to the diffusion [119]. Here, the Damköhler number is measuring this ratio for the thermally excited, mobile electrons ($\theta_{e,mobile}$), and is defined as:

$$Da = \frac{k_1 s^2}{D_e}, \tag{4.28a}$$

where the reaction rate coefficient is:

$$k_1 = \eta\left(\frac{v_e}{\lambda_{trap}}\right)\exp\left(-\frac{\Delta H_{eff}}{k_b T \omega_e}\right). \tag{4.28b}$$

A large Damköhler number (>>1) characterizes a fast reaction, inducing a reaction concentration gradient, while a slow Damköhler number (<<1) designates a slow reaction, resulting in a uniform concentration [119]. Typically, the Damköhler number is a constant for a given system at a specific set of conditions. Here, *Da* will change throughout the dielectric stress due to the time-dependence from D_e and k_1. Therefore, *Da* can be measured as functions of time, electric field, and dielectric thickness. The electron temperature is transformed into:

$$\omega_e = 1 + \frac{2V_{app}\lambda_{op}}{3V_T s}\psi, \tag{4.28c}$$

where ω_e represents the ratio of the electron temperature to the substrate temperature. At common nominal electric fields, this ratio increases as the optical scattering length (λ_{op}) increases or thermal energy decreases.

An important advantage to dimensionless equations is variable scaling. As previously discussed, the length scales from 0 to 1, as do the electron and defect density variables. This is also true for the boundary conditions and initial conditions. The boundary conditions for the voltage and mobile electrons are expressed as:

$$\upsilon(\xi = 0, \tau) = 0, \tag{4.29}$$

$$\upsilon(\xi = 1, \tau) = 1, \tag{4.30}$$

$$\theta_{e,mob,total}(\xi = 0, \tau) = \exp\left(-\frac{\phi_{B,eff}}{qV_T}\right), \tag{4.31}$$

and

$$\theta_{e,mob,total}(\xi = 1, \tau) = 0. \tag{4.32}$$

The initial conditions are defined as:

$$\theta_{e,mob,total}(\xi, \tau = 0) = 0, \tag{4.33}$$

$$\theta_{e,trapped}(\xi, \tau = 0) = 0, \tag{4.34}$$

and

$$\theta_{trap}(\xi, \tau = 0) = \frac{C_{trap,0}}{N_{e,metal}}. \tag{4.35}$$

Although the model requires experimental data to determine three parameters (A_{eff}, Φ_B, and η), the theoretical results from the dimesionless equations will be presented before the comparison between the model and experimental data, in order to provide a framework for the behavior of the dielectric breakdown process. The model parameters used in this section are the same as the parameters used in Section 4.2, unless otherwise noted. A complete summary of the model parameters is listed in Table 4.1. Simulations were run at nominal electric fields ($E=V_{app}/s$) between 5 and 7 MV/cm, and dielectric thicknesses ranging from 5 nm to 30 nm.

The Péclet number, as shown in Equation 4.25b, is directly proportional to the dielectric thickness. Figure 4.1A shows this relationship based on simulations at different dielectric thicknesses. The *Pe* values used here were taken during initial electrical stress, where $\tau \sim 1$. Even at 5 nm, $Pe \sim 20$, indicating convective-dominated electron transport. Thus, there is no expected electron concentration gradient across the dielectric position due to mass transport behavior. The Péclet number also evolves over time in this system due to the time-dependence of the electron velocity and diffusion coefficient. Figure 4.1B shows the progression of the Péclet number as a function of the time constant at different nominal electric fields, for a dielectric thickness of 5 nm. As the dielectric accumulates defects, *Pe* starts to increase. This increase sharpens through the breakdown process, mimicking the abrupt increase in current seen at failure. Thus, as the dielectric wears out and fails, convective transport becomes even more dominant over diffusion-driven transport. Figure 4.1B also shows that *Pe* is not a strong function of the electric field at initial stress times.

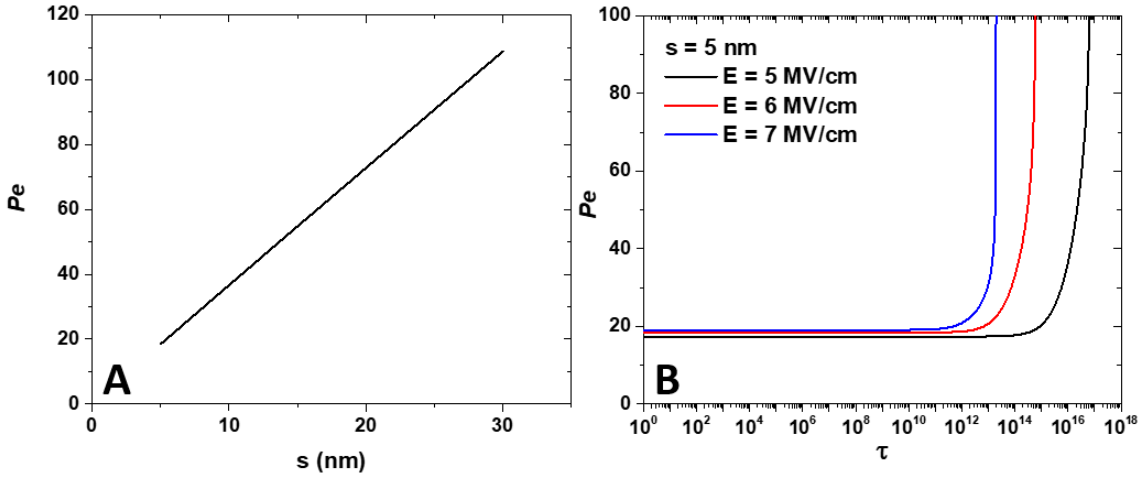

Figure 4.1. Analysis of the Péclet number for mobile electrons. A) *Pe* is directly proportional to the dielectric thickness and is >>1 for dielectric thicknesses 5 nm and above, indicating convective-dominated transport. B) As dielectric breakdown progresses, *Pe* increases to greater than 100.

The Damköhler number can also provide an indication if an electron concentration gradient will occur, based on the reaction kinetics of the electrons interacting with new, empty defects. In this model, electron trapping is assumed to be favorable, such that newly generated defects immediately trap an electron. Thus, if the reaction rate to generate defects is fast relative to the electron diffusion, an electron concentration gradient will develop. Defects are immobile in the dielectric, so this Damköhler number is not relevant to determine any concentration gradient for the traps.

The Damköhler values as a function of dielectric thickness, based on simulation results, are shown in Figure 4.2A. Overall, *Da* is <<1, indicating a slow reaction. As the dielectric thickness decreases, the Damköhler number also decreases. Therefore, the reaction is slowing down for thinner dielectrics, which will results in an increase in failure time. Figure 4.2B shows the progression of *Da* as a function of the time constant at several electric fields. Similar to *Pe*, the Damköhler number increases as the reaction plays out and new defects are generated. This can be partially attributed to the decreasing diffusion coefficient, which is inversely proportional to *Da*. At noted in the previous chapter, a defect density of ~1 x 10^{25} atoms/m^3 is required to start the breakdown process, which is 4 orders of magnitude smaller than the maximum allowed

trap density ($C_{trap,max}$) that serves to limit the defect reaction rate. Thus, breakdown occurs before the reaction can be slowed down by its self-limiting term.

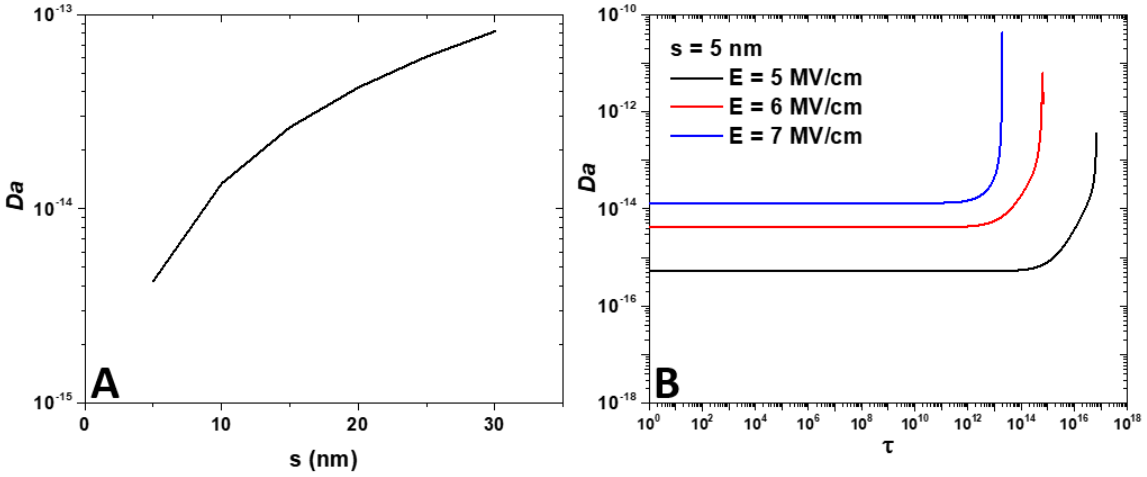

Figure 4.2. Analysis of the Damköhler number for mobile electrons. A) *Da* decreases as a function of the dielectric thickness and is <<1, indicating slow reaction kinetics to generate new defects. B) As defects are generated, *Da* increases, although still with slow reaction kinetics throughout the breakdown process.

Based on the analysis of the Péclet and Damköhler numbers, no electron concentration gradient is expected across the dielectric due to mass transport or reaction kinetics, respectively. The mobile electron density is shown in Figure 4.3 as a function of the dimensionless length for various dielectric thicknesses. As expected, the mobile electron concentration is constant across the dielectric position, with the exception of $\xi >$ 0.95, where the density decreases sharply. This is due to the $\theta_{e,mob,total}$ boundary condition at the anode, which was intentionally set equal to zero to ensure the electron flux was not limited at this electrode. Overall, the concentration gradient occurs over a small fraction of the dielectric (<5%), with most of the gradient occurring in less than 1% of the dielectric.

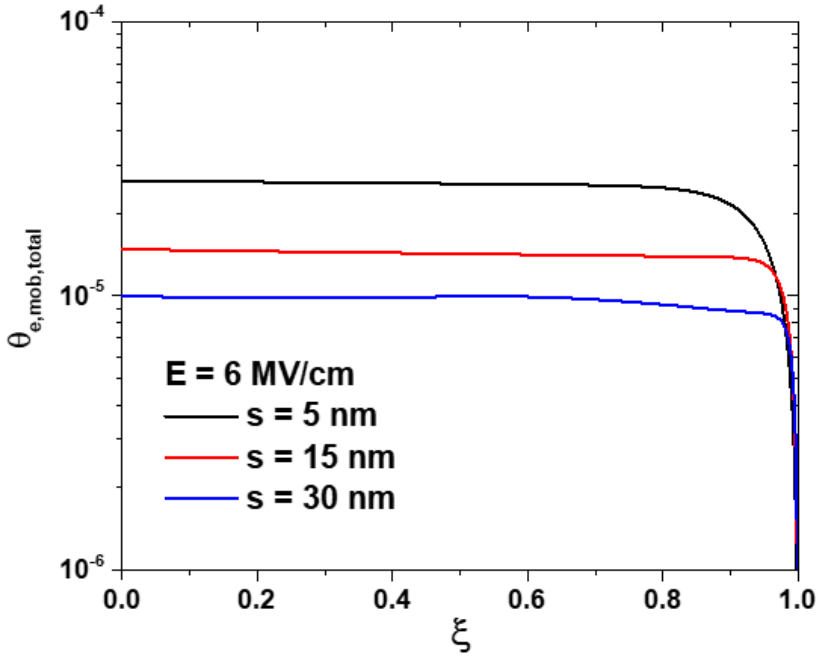

Figure 4.3. Mobile electron density from simulations at a nominal electric field of 6 MV/cm for various dielectric thicknesses. Consistent with analysis of *Pe* and *Da*, the mobile electron density is constant throughout the dielectric position, except near the anode where the boundary condition is intentionally set equal to zero to ensure no electron flux limitations.

The local electric field (defined here as ψ) is an extremely important variable to understand because most other variables are dependent to ψ. Therefore, ψ can be examined as a function of the nominal electric field, dielectric thickness, and time constant to gain an improved understanding of various dielectric behaviors. Figure 4.4A shows ψ as a function of the dimensionless position for dielectric thicknesses of 5 nm, 15 nm, and 30 nm at a nominal electric field of 6 MV/cm. The first main takeaway is that the local electric field is lower at the cathode relative to the anode, indicating a buildup of negative charge in the dielectric. The second takeaway is that the ψ-ξ slope decreases for thinner dielectrics at 6 MV/cm. With a negative charge buildup in the dielectric, this reduced slope causes a higher local electric field at the cathode for thinner dielectrics. However, if the overall charge in the dielectric were positive, this trend would be reversed. This higher electric field at the cathode for thinner dielectric is relevant to electron injection, and explains why the mobile electron density is larger for

thinner dielectrics in Figure 4.3. The lower ψ-ξ slope for thinner dielectrics can be attributed to Q, which scales according to s/E. Thus, Q decreases for thinner dielectrics relative to thicker dielectrics, when compared at the same nominal electric field. The other term that can influence the ψ-ξ slope is the overall charge in the dielectric. Although this is shown in Figure 4.4B to become more negative for thinner dielectrics (due to the increased concentration of mobile electrons), Q must have a larger thickness dependence compared to θ_{charge}, in order to explain the electric field trends in Figure 4.4A.

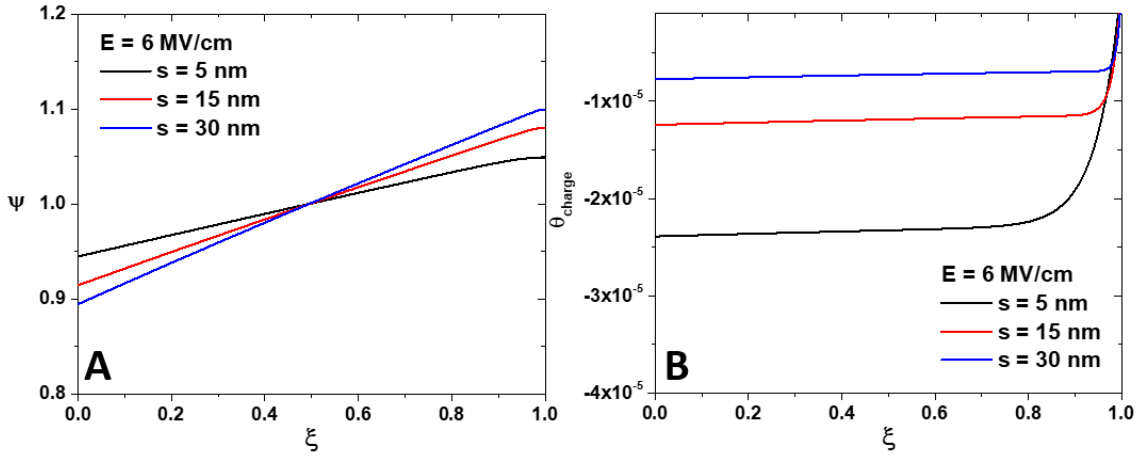

Figure 4.4. A) Local electric field as a function of dielectric position for different thicknesses, shows a higher electric field at the cathode for thinner dielectrics. B) Overall charge in the dielectric as a function of dielectric position for different thicknesses, shows thinner dielectrics have a larger buildup of negative charges at E = 6 MV/cm, which is due to a higher density of mobile electrons.

These electric field trends have been shown at a relatively high nominal electric field (E = 6 MV/cm), where there is a higher density of mobile electrons relative to initial, positively-charged defects. However, as E decreases, the mobile electron concentration also decreases, and there should be a cross-over point where the overall buildup of charges in the dielectric becomes positive. Figure 4.5 shows how the local electric field at the cathode changes as a function of the nominal electric field for 5 nm and 30 nm thick dielectrics. This cross-over point can be observed just below a nominal electric field of 5 MV/cm. At higher E, ψ is larger for thinner dielectrics relative to thicker dielectrics, but below this cross-over point, ψ becomes smaller for thinner

dielectrics versus thicker dielectrics. This can create interesting failure trends near this cross-over point, where the local and nominal electric fields are not changing at the same rates for dielectrics of different thicknesses.

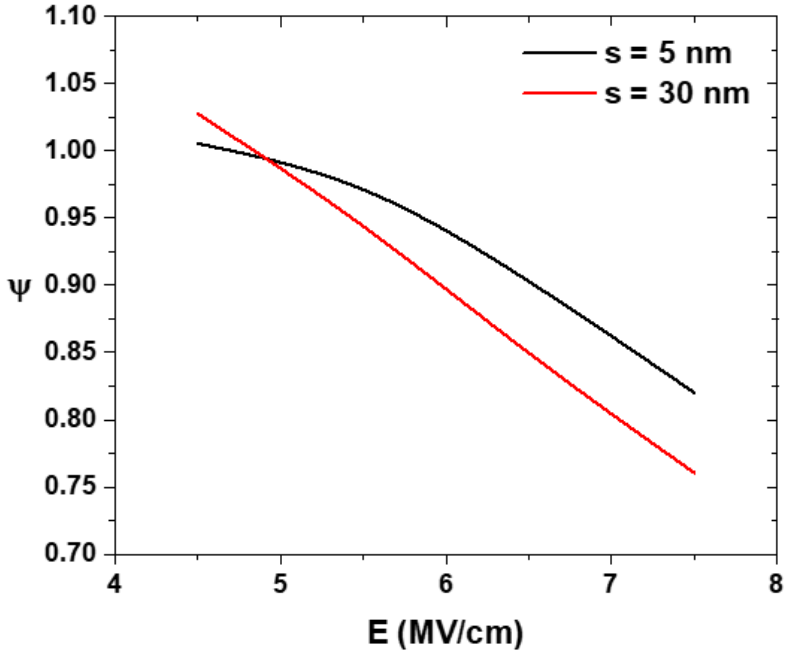

Figure 4.5. Local electric field (ψ) at the cathode as a function of nominal electric field for 5 nm and 30 nm thick dielectrics. ψ = 1 represents where the local electric field equals the nominal electric field, corresponding to neutral overall charges in the dielectric. Thinner dielectrics experience a higher ψ at high nominal electrics fields compared to thicker dielectrics, but this trend reverses just below E = 5 MV/cm, where positively-charged defects outnumber electrons in the dielectric.

Figure 4.6 shows the progression of ψ (near the cathode) during electrical stress at different nominal electric fields. During the dielectric failure process, ψ increases sharply. This originates from the tunneling electrons, leaving behind empty traps with positive charges. The time at which ψ increases above a value of 1 is when the positive charges exceed the negative charges in the dielectric. The increase in the electric field at the cathode results in more electrons being injected, further increasing the defect generation rate, and creating a feedforward failure process.

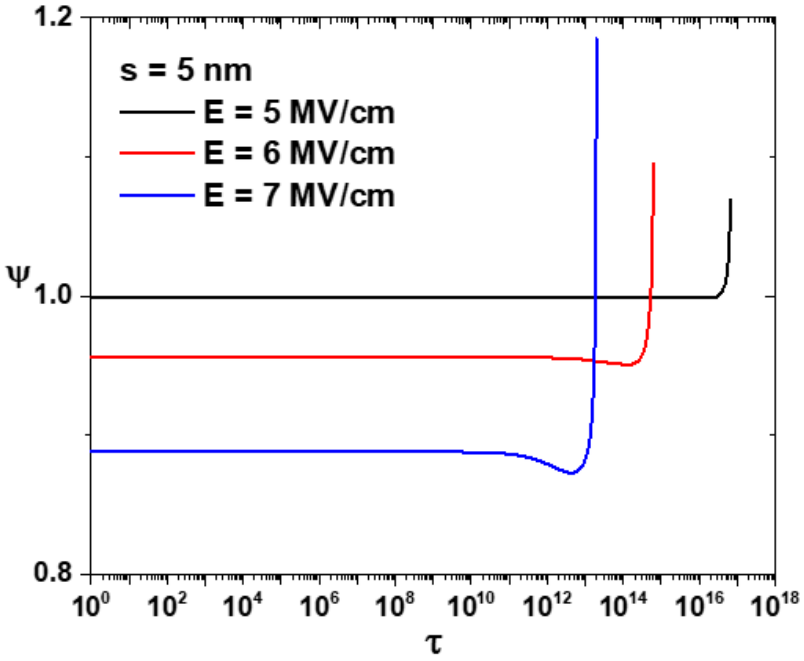

Figure 4.6. Local electric field, measured at the cathode, as a function of the time constant at various electric fields, shows an abrupt increase for failure.

A thinner dielectric has been shown to decrease the convection transport relative to diffusive transport, slow down the defect generation reaction, and increase the electric field at the cathode, which increases the mobile electron density in the dielectric. Despite the increased concentration of mobile electrons, Figure 4.7 shows the overall electron flux decreases as the dielectric thickness decreases. This is attributed to the decreasing Péclet number, which is directly proportional to the convection component of the electron flux and shown to be the dominant mode of electron transport. Thus, an overall decrease in the current can be expected for thinner dielectrics, despite a higher mobile electron concentration. It should be noted that the model is only set up to observe intrinsic conduction following Schottky emission or Poole-Frenkel conduction. Tunneling mechanisms and extrinsic issues (such as copper) that become more important for thinner dielectrics would serve to counter-act this trend and cause a higher leakage current.

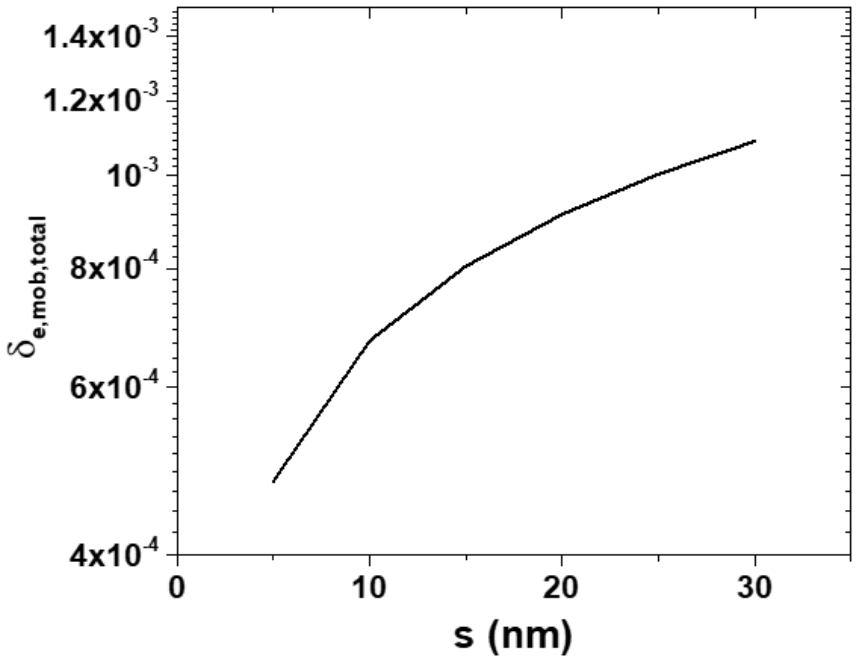

Figure 4.7. Electron flux as a function of dielectric thickness. The flux decreases for thinner dielectrics, which can be attributed to a smaller Péclet number.

The defect generation rate is a very strong function of the electric field, which was shown to be non-constant across the dielectric position. Since defects are immobile in the dielectric, defect concentration gradients can form based on non-uniformity of the electric field. Figure 4.8 shows the defect density across the dielectric at three different time stages: initial stress (black line), the start of the increase in electron flux due to failure (red line), and near the failure time (blue line). The purpose is to show the evolution of the defects through the dielectric. Initially, as defined by the equations, the defect density is constant across the dielectric. However, the electric field is higher near the anode relative to the cathode, creating defects faster near the anode. Therefore, trap-to-trap electron tunneling will occur near the anode first where the defect density is highest, and then progress to the cathode, creating failure. The defect density acts as a moving front, from the anode to the cathode.

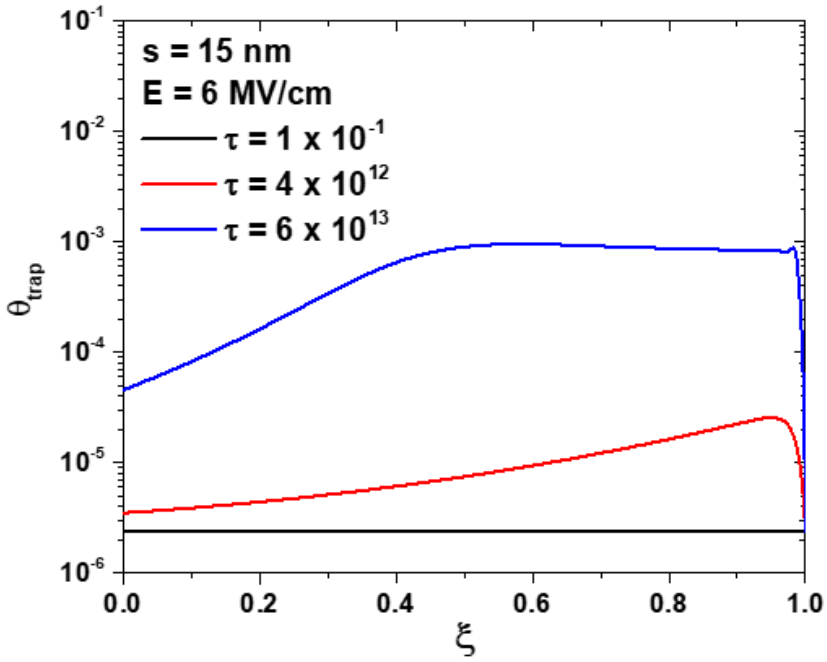

Figure 4.8. Defect density as a function of the position in the dielectric at three different times: early stress (black line), beginning of the dielectric failure (red), and near the failure time (blue). Defects grow faster near the anode, and create a moving front towards the cathode to cause failure.

The defect scattering length (λ_{trap}) is directly related to the defect density, such that as the defect density increases, λ_{trap} decreases. The dielectric failure process initiates when λ_{trap} decreases to a value small enough for trap-to-trap tunneling to occur. Figure 4.9 shows the evolution of the defect scattering length as a function of time at various nominal electric fields. The initial defect scattering length is approximately 5 nm. This value stays constant through the electrical stress until the last decade of two before the failure time. First, the scattering length decreases slowly, but this is quickly accelerated as defect generation increases and the feed-forward failure mechanism occurs. At the highest simulated field (7 MV/cm), this acceleration process is quick, as trap-to-trap tunneling is increased at higher fields. For the lowest simulated field (5 MV/cm), the decrease in λ_{trap} is slower, as the electrons cannot as easily escape the defects. At each simulated field, the failure time corresponds to a defect scattering length of approximately 1 A°, or 50 times smaller than the initial scattering length.

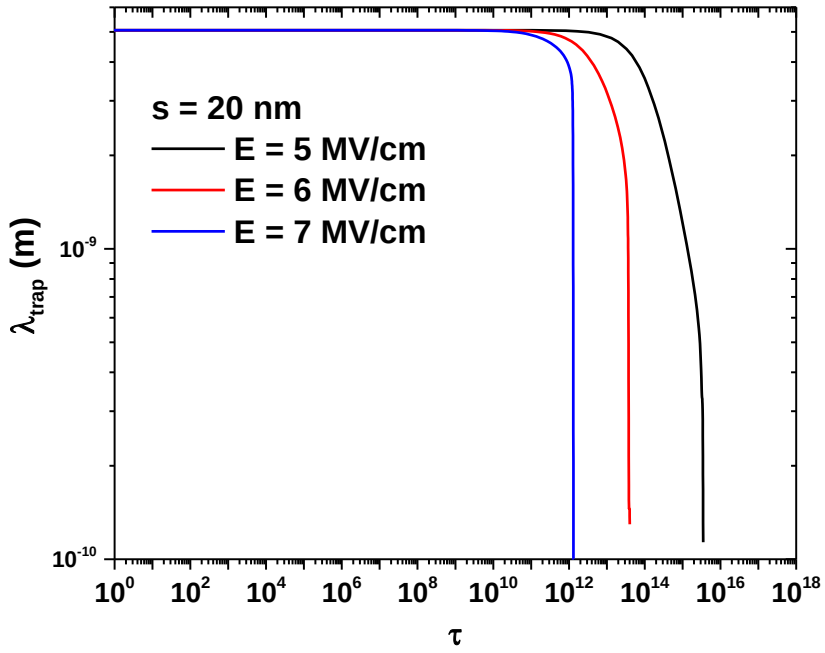

Figure 4.9. Scattering length as a function of stress time at three different electric fields. At the dielectric failure time, the scattering length is approximately 1 A°.

Last, the re-defined electron temperature is examined in its dimensionless form. The electron temperature previously decayed as defects accumulated in the dielectric, but this new form is solely dependent on the local electric field and the substrate temperature. Figure 4.10 shows the electron temperature relative to the substrate temperature (ω_e) as a function of the nominal electric field for 5 nm and 30 nm dielectric thickness, measured near the cathode. ω_e increases as the nominal field increases, as expected. However, at higher nominal fields, the 5 nm dielectric has a slightly higher electron temperature compared to the 30 nm dielectric. This follows the same trend as the local electric field shown in Figure 4.5. Thinner dielectrics have a higher electron temperature at high nominal fields when there is a net negative charge in the dielectric. But, near E = 5 MV/cm, where the overall net charge is close to zero, the 5 nm and 30 nm thick dielectrics have similar electron temperatures. Although a higher electron temperature would increase the defect generation rate, this term is already included in the Damköhler number, which was shown to decrease for thinner dielectrics.

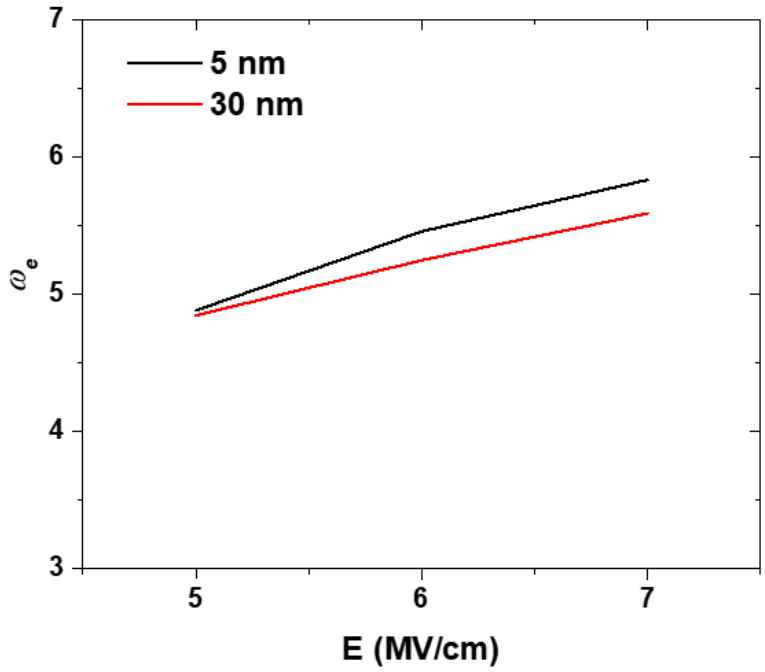

Figure 4.10. Dimensionless electron temperature as a function of electric field for 5 nm and 30 nm dielectrics.

4.2 Comparison to Experimental Data

The dimensionless analysis explained how several of the most important variables behave for various dielectric thicknesses and testing conditions. This analysis will be helpful to explain some of the experimental data shown in this section. The dimensional form of the equations are used here to fit to the experimental data, and explain dielectric failure for low-κ SiCOH as a function of voltage, temperature, and dielectric thickness.

4.2.1 Test Methodology

Tests were conducted on multiple wafers from GLOBALFOUNDRIES using their 14 nm technology. Via-chain and comb-comb structures were used, where the dielectric consisted of low-κ SiCOH with a dielectric constant κ = 2.7.

For voltage ramp tests, 32 to 64 chips were tested on each wafer, with 20 identical test structures on each chip. Voltage ramp (V_{ramp}) tests were conducted on the

samples at 125 °C using a ramp rate of 1 V/s. Breakdown was defined as the last applied voltage before the current exceeded a threshold of 1 x 10^{-5} A.

For CVS tests, 16 chips were tested on each wafer per voltage condition, stressing between 1 to 10 identical test structures per chip. Tests were conducted on the samples at a temperature between 85 °C and 125 °C. Breakdown was defined as the last measured time before the current exceeded a threshold of 1 x 10^{-5} A.

4.2.2 Parameter Estimation and Voltage-Dependent Failure Prediction

The model relies on three parameters (A_{eff}, Φ_B, and η) to generate the electrical traces for comparison to the experimental data. These parameters, like all of the parameters incorporated into the model, are based on the properties of the intrinsic dielectric material and how that material relates to the breakdown process. The details of the parameter estimation have been previously discussed [103], [111]. A_{eff} and Φ_B are determined based on the relationship between current and voltage, either an *I-V* curve from a voltage ramp test or leakage current at different electric fields from a CVS test. A_{eff} is determined based on the overall magnitude of current, while the *I-V* slope is used to set Φ_B. Here, η is fixed based on the failure time from a single voltage for a CVS test. It can also be determined based on the breakdown voltage from a voltage ramp test.

Figure 4.11 shows the *I-V* curve for a voltage ramp test, and the corresponding fit by the model. The current increases with an exponential dependence on the voltage, until an abrupt jump occurs, indicating breakdown. The model shows similar behavior, with a few key differences. At low voltages, the *I-V* slope deviates ~15% between the experiment and the simulation. This could indicate a different conduction mechanism dominates at lower voltages. Another possibility is that ε_∞, which controls the *I-V* slope at low voltages, is incorrect. ε_∞ is estimated based on a relationship to κ [73], resulting in some uncertainty in its proper value. At high voltages, the leakage current continues to increase steadily, while the model predicts a saturation before the breakdown event occurs. This is most likely associated with the definition of the electron velocity, which is limited by the defect density. As the defect density increases, the electron velocity decreases, causing the current to saturate. However, previous experimental *I-V* curves have also shown this saturation behavior [111], indicating this equation is correct in

some cases. Although the simulation does not provide a perfect prediction of the experimental *I-V* curve, it yields a satisfactory fit, especially in the voltage range for which CVS tests were conducted.

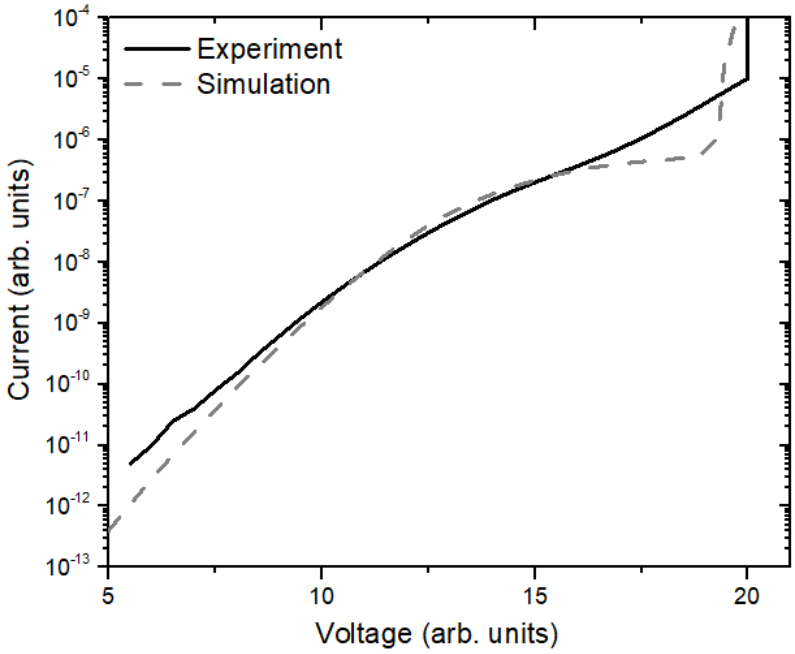

Figure 4.11. Current as a function of voltage for a voltage ramp test at 125 °C. Although the simulation (dash line) deviates from the experimental data (solid line) at the lowest and highest voltages, the model provides a sufficient fit to the data to predict failure for CVS tests shown in Figure 4.12.

Figure 4.12 shows the results of the CVS tests conducted at 125 °C. These tests were carried out over a wide range of voltages, and therefore, the failure times vary from several minutes at high-field to several months at low electric fields. Overall, the charge transport model provides an excellent fit to the failure times, despite not using any parameters to change the TTF-Voltage slope. The simulations start to over-predict the failure at the highest voltages tested, but this can be attributed to the model under-predicting the leakage current at the high voltages, as seen in Figure 4.11. This serves to demonstrate the main basis for the charge transport model, which is that the dielectric breakdown process is strongly tied to the electronic conduction. The model is only

useful to predict failure in the ranges where it can also accurately predict the leakage current.

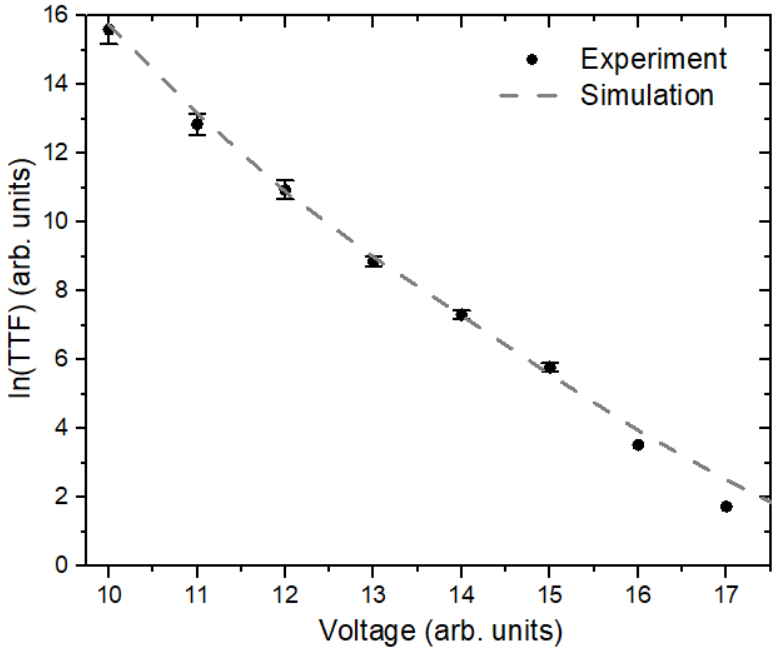

Figure 4.12. Average time-to-failure (TTF) as a function of voltage. Experimental data (circles) and simulation results (dash line) match very well, except at high voltages where the model is also unable to predict the leakage current.

An analysis of the three adjustable parameters (A_{eff}, Φ_B, and η) can provide useful information about the model and the material properties. Φ_B is the energy barrier for electron injection into the dielectric. For integrated structures, such as the comb-comb and via-chain structures measured in this paper, the lowest energy barrier for electrons to enter the dielectric is most likely at the interface between the metal barrier and the etch stop layer (TaN/SiCN:H) [32]. The energy barrier at this interface was measured to be in the range of 1.45 eV to 2.15 eV [32], [104], which is consistent with Φ_B = 1.58 eV used in these simulations.

A_{eff} and η are necessary to account for conduction and breakdown that occur only through a very tiny fraction of the dielectric [69]. This can also be described as failure at one of several hotspots, or weak points, in the material. A_{eff} is the effective area through which electronic conduction occurs, and is used to convert the electron flux into current

for the one-dimensional simulations. It was previously shown that $A_{eff} = A*P_{eff}$, where A is the area of the test structure and P_{eff} is the fraction of the dielectric through which conduction occurs, with $P_{eff} = 5 \times 10^{-10}$ [111]. In this simulation, $A_{eff} = 2 \times 10^{-18}$ m^2, but the area of the test structure is unknown so P_{eff} cannot be calculated. A_{eff} matches closely to previous simulations carried out for low-κ SiCOH using the charge transport model [103]. η is part of the defect generation equation and represents the fraction of the dielectric through which defect generation is occurring. In these simulations, $\eta = 1 \times 10^{-11}$, which is ~50x smaller than P_{eff} in previous simulations for SiN [111], indicating that the electron conduction and defect generation may be closely related to each other. The smaller η could be a result of the different materials, or an indication that defect generation occurs in an even smaller fraction of the dielectric compared to the electronic conduction. η is also the last parameter to be set in the simulations, so it takes on any parameter errors that might affect the failure time. This results in a larger uncertainty in its value. Further exploration of these parameters relationship to each other is required, and future work to extend this model to 2-D may also provide some insight about the nature of these parameters. A summary of the model parameters used in the simulations is listed in Table 4.1. Summary of model parameters set by the experimental conditions and material properties, including the source of the parameter value where appropriate..

Table 4.1. Summary of model parameters set by the experimental conditions and material properties, including the source of the parameter value where appropriate.

Parameter	Value	Reference
A_{eff}	2×10^{-18} m^2	Fit to Data
$C_{trap,0}$	2.0×10^{23} m^{-3}	[74]
$C_{trap,max}$	1.0×10^{29} m^{-3}	Calculated
E_p	0.070 eV	[118]
Φ_{trap}	1.2 eV	[20]
L	0.88	[109]
m_e^*	$0.5m_e$	[50]
$N_{e,metal}$	8.5×10^{28} m^{-3}	[68]
s	27 nm	Calculated
α	7 eA$^{\circ}$	[112]
ΔH	3 eV	[42]
ε_∞	2.2	[73]
η	1×10^{-11}	Fit to Data
κ	2.7	Measured
Φ_B	1.58 eV	Fit to Data

4.2.3 Temperature-Dependent Failure Prediction

The activation energy for dielectric failure was investigated through CVS tests, conducted at several electric fields and various temperatures. Simulations were also run at similar conditions, shown in Figure 4.13A. Although subtle, the model shows a higher temperature dependence for dielectric failure at lower electric fields compared to higher fields. This is further exemplified by fitting both the experimental and simulation failure times to an Arrhenius relationship in order to calculate the dielectric failure activation energy at each electric field, shown in Figure 4.13B. The test data shows the activation energy increases as the electric field decreases. The simulation results show the same trend, agreeing well with the experiments. These results are consistent with previous TDDB activation energy studies [49]–[52].

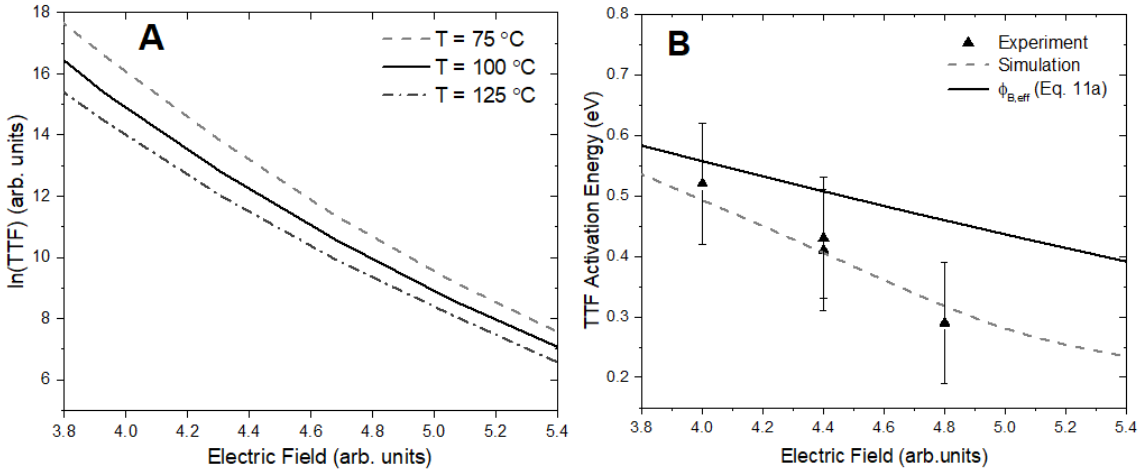

Figure 4.13. Calculation of the activation energy for dielectric failure. A) Simulations at three different temperatures and at different electric fields and B) TTF activation energy predicted by the Arrhenius relationship shows an increasing activation energy for decreasing electric field. The experimental data (triangles) and simulations (dash line) show excellent agreement, and the cause of this trend is attributed to the electron conduction energy barrier.

The cause for this trend is due to the electron injection process into the dielectric (Equation 4.11). The electrons need to overcome an energy barrier at the cathode (Φ_B), and this barrier is lowered by the electric field ($\Phi_{B,eff}$). This effective energy barrier is plotted in Figure 4.13B, as a function of the nominal electric field (V_{app}/s). $\Phi_{B,eff}$ actually predicts a larger activation energy compared to the experimental data and simulation. The difference is caused by the local electric field at the cathode, which is higher than the nominal electric field due to the positively charged defects present in the dielectric. The difference between $\Phi_{B,eff}$ and the model predictions can be attributed to the other temperature dependent terms in the model, which act to reduce the overall activation energy for failure. Notably, the defect scattering length (λ_{trap}) increases as temperature increases, decreasing the defect generation rate and increasing the defect density required for failure.

For chips that operate at lower temperatures than testing conditions, the selection of the activation energy can have dramatic implications on lifetime prediction. To demonstrate this, a lifetime improvement factor (LIF) is calculated for several activation energies at different operating temperatures, based on a testing condition of 125 °C. The

results are shown in Table 4.2. For an activation energy of 0 eV, the lifetime is unaffected by the operating temperature of the chip. For 0.4 eV, which represents the average activation energy from the experimental data in Figure 4.13B, the lifetime of the chip can be improved 5x if the chip operates at 75 °C. For 1.0 eV, calculated using Equation 4.11a at an operating field of 1 MV/cm, the chip lifetime improves 7x at 100 °C and 66x at 75 °C. Clearly, the activation energy for dielectric failure is an important TDDB parameter that can have a large effect on lifetime prediction.

Table 4.2. Lifetime improvement factor (LIF) calculated at various activation energies and operating temperatures. An activation energy of 1.0 eV can provide a 66x boost in lifetime prediction for a chip that operates at 75 °C compared to 125 °C testing condition.

Activation Energy	**LIF**	
	T_{op} = 100 °C	**T_{op} = 75 °C**
0 eV	1	1
0.4 eV	2	5
1.0 eV	7	66
Sim + $E^{1/2}$ Model	7	126

For comparison, the simulation results at each temperature were fitted to the $E^{1/2}$ model in the same electric field range as the experiments. The purpose is to calculate the dielectric lifetime based on experiments at different temperatures (the simulation results were used instead of the experimental results to remove experimental uncertainties). The choice of empirical lifetime model is not important for this study. Due to the voltage-acceleration dependence to the activation energy, lower temperature tests yield a larger voltage-acceleration slope compared to tests at higher temperatures. The same lifetime improvement factor analysis was used for the $E^{1/2}$ model predictions, and the results are shown in Table 4.2. This approach predicts similar lifetime improvement as the Arrhenius equation with an activation energy of 1 eV. Two conclusions can be drawn from this analysis. First, 1 eV is a more accurate activation energy for dielectric failure at an operating field equal to 1 MV/cm compared to the experimental values ranging between 0.3 eV and 0.5 eV). Second, it is beneficial to test dielectric failure at the same

temperature as the product operating condition, rather than extrapolate from a high temperature test using a conservative activation energy less than 1 eV.

4.2.4 Failure Distributions Prediction

Dielectric failure variation can be caused by many contributing factors. However, in the advanced technology nodes where the dielectric thickness is only tens of nanometers thick, control of the thickness is considered to be the main driver for failure. These thickness variations are caused by manufacturing steps, such as lithography, etch, and chemical mechanical planarization (CMP) [25], [120]. Line-edge-roughness (LER) causes local spacing variations, which typically manifest as protrusions and notches along the dielectric-metal interface and cause non-uniform fields [25]. Line overlay and via-misalignment are global issues [26], causing a variation in the dielectric thickness amongst samples across a wafer. Typically, breakdown in the interconnect will occur through the dielectric at a via-line location [27], although line overlay and LER can further decrease the spacing at this location to accelerate the breakdown. Dielectric spacing variation has been addressed since the 90- and 65-nm technology nodes [25], and it is expected to be the dominant cause of failure deviation for current and future technology nodes. As a result, early-population failures are dominated by the smallest spacing samples [28], [29].

4.2.4.1 Method to Determine the Root Cause of Failure

For integrated structures, dielectric thickness is not an easily measurable parameter like voltage and temperature. Thus, it must be calculated. Further, a method is required to prove that dielectric thickness variations are the main driver for the failure distributions. In this section, a novel method is presented to determine the dominant parameter affecting failure distributions within a group of samples [121]. This method analyzes voltage ramp (V_{ramp}) data, measuring differences in leakage current and breakdown voltages between test structures spread across a wafer or located within a specific chip on a wafer.

The method used in this paper is relatively straightforward; the variation in the V_{ramp} leakage current (I) between samples was analyzed as a function of the voltage (V)

and as a function of the electric field (E). In order to define the electric field, an assumption is made that the dielectric spacing (s) is the dominant parameter that controls the V_{ramp} failure distribution. Based on this assumption, the dielectric spacing for each sample was calculated based on the breakdown voltage (V_{BD}) from each V_{ramp} test using $s=V_{BD}/E_{BD}$ [27], [29]. Here, E_{BD} is the breakdown strength of the dielectric, determined to be 0.75 V/nm [29]. The validity of this assumption can be re-assessed based on the results. The samples were grouped in two ways for data analysis: 1) samples located on 64 different chips on a wafer (across-wafer), and 2) samples on the same chip (in-chip).

The logarithmic value of the leakage current, denoted as *log(I)*, was used so that all data was weighted equally. For a group of samples, the standard deviation of *log(I)*, denoted as $log(I)_{StdDev}$, was calculated at common voltages or electric fields. Analysis was started when all samples in a group measured a leakage current above a minimum threshold ($I > 5x10^{-11}$ A), and analysis was stopped when the first sample in a group failed. This minimized error related to the equipment noise or associated with the failure of a sample.

It is prudent to start with the ideal case that the only difference between samples in a group is their dielectric spacing, which dictates each sample's *I-V* trace and breakdown voltage. Then, two trends will be observed in the method's results. First, $log(I)_{StdDev}$ analyzed as a function of voltage will have a value greater than zero, and will show a significant increase as the voltage increases and approaches the breakdown voltage. At common voltages, the samples are actually at different electric fields, and will exhibit different leakage currents. This trend becomes more prevalent at higher voltages as the thinner samples approach their breakdown voltage while the thicker samples are not as close to failure. Second, $log(I)_{StdDev}$ analyzed as a function of electric field will be zero. If the dielectric spacing is truly the only varying parameter between samples, then the samples' *I-E* traces will be identical.

Figure 4.14 shows the method's results for across-wafer sample grouping. Two wafers were analyzed (labeled as 1 and 2), and the $log(I)_{StdDev}$ analysis is shown both as a function of voltage (red) and as a function of electric field (black). There is a clear increase in the voltage-analyzed $log(I)_{StdDev}$ values above 15 V as the voltage increases. The increasing trend is expected to continue at higher voltages as well, but the analysis

was stopped at the lowest breakdown voltage amongst the samples. This is the first indication that the dielectric spacing varies between samples across the wafer, and is the dominant parameter responsible for the failure distribution amongst these samples. This is consistent with the results from previous studies showing the dielectric thickness varies between samples across a wafer [122], [123].

This is further validated by the field-analyzed $log(I)_{StdDev}$ values, which are lower compared to voltage-analyzed $log(I)_{StdDev}$ values. These smaller values show that the correction using the electric field, calculated by the dielectric spacing, is appropriate. Although the *I-E* leakage traces would ideally be identical between samples, in reality there are still small variations between samples' leakage current due to several factors. These factors include error in calculating V_{BD} (±0.1 V, which leads to ±0.13 nm error in *s*), error in measuring the current, and differences between in-chip samples, which will be discussed next.

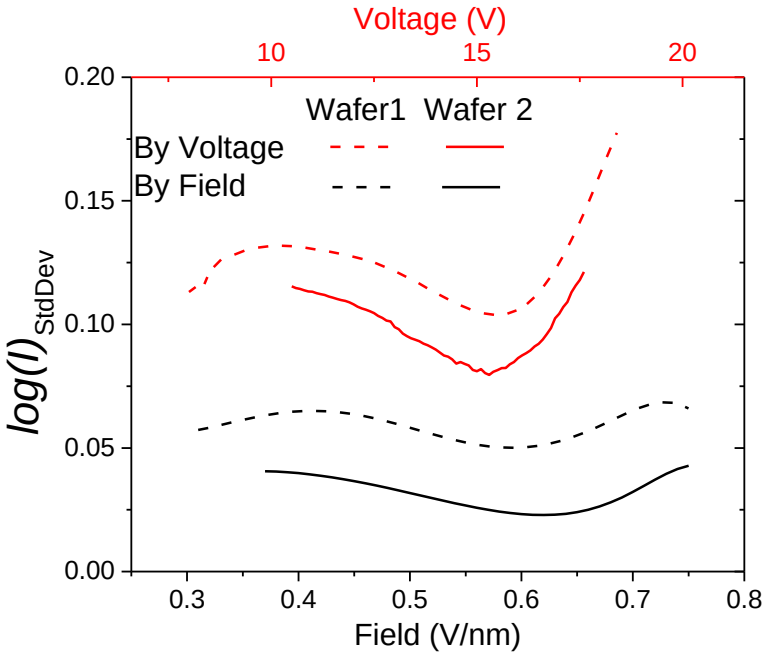

Figure 4.14. Current variation for across-wafer samples, analyzed as a function of voltage (red) and electric field (black). The results indicate that spacing variation dominates V_{ramp} failure distributions.

The method's results for the in-chip sample grouping are shown in Figure 4.15. The analysis for two chips are shown (located in the center of the wafer, or on the edge of the wafer), and the $log(I)_{StdDev}$ analysis is shown both as a function of voltage (red) and as a function of electric field (black). The field-analyzed $log(I)_{StdDev}$ values are higher than the voltage-analyzed $log(I)_{StdDev}$ values, regardless of the chip location. These in-chip results sharply contrast the across-wafer results in Figure 4.14. The field-analyzed $log(I)_{StdDev}$ values for the in-chip samples significantly increase at high electric fields, echoing the voltage-analyzed trends for the across wafer samples. These trends indicate that correcting for the dielectric spacing is not a valid assumption for in-chip samples. Therefore, in-chip failure distributions are not dominated by the dielectric spacing.

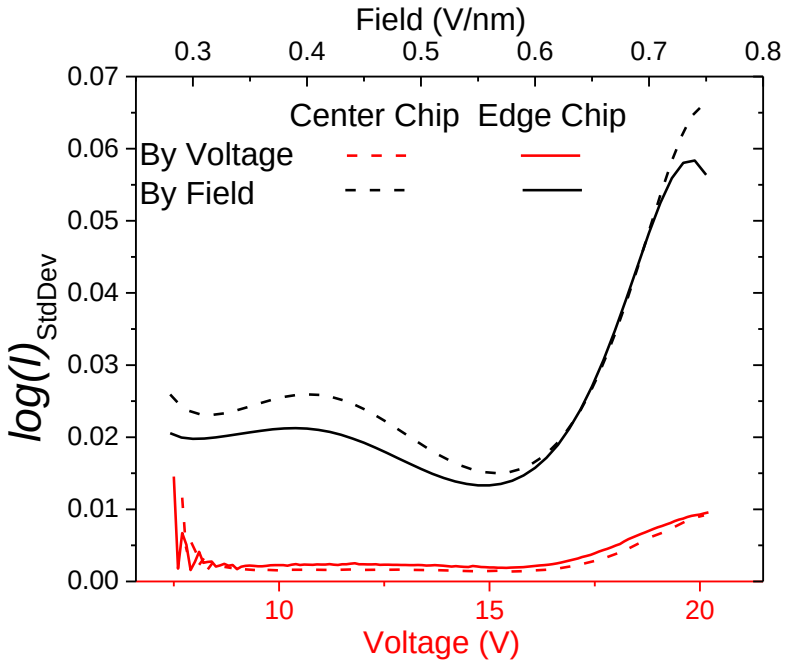

Figure 4.15. Current variation for in-chip samples, analyzed as a function of voltage (red) and electric field (black). The results indicate that spacing variation does not dominate V_{ramp} failure distributions.

Line overlay and via misalignment are global issues (affecting dielectric thickness between samples across a wafer), while LER is a local issue (affecting thickness within a sample). Therefore, the dielectric spacing variations between across-wafer samples can be attributed to line overlay and via misalignment (and more likely

via misalignment for the via-comb structures in this study). Although LER could possibly manifest between in-chip samples, Figure 4.15 shows this is not the case. LER most likely still occurs and decreases the overall dielectric thickness of each sample, but the effect of LER is the same between all in-chip samples.

Thus far, it has been shown that comparing voltage-analyzed $log(I)_{StdDev}$ values and field-analyzed $log(I)_{StdDev}$ values can indicate whether or not spacing dominates the failure distribution. Figure 4.16 represents another way to display this analysis; the minimum $log(I)_{StdDev}$ value is calculated for each sample group and plotted as a function of field vs. as a function of voltage. The dash line represents a one-to-one ratio; below the line represents spacing dominated failure and above the line indicates the failure is dominated by some other parameter. Figure 4.16 provides an easy visual to analyze different groups of samples, and this visual provides the same conclusions drawn from Figure 4.14 and Figure 4.15; spacing dominates across-wafer failure, but not in-chip failure.

After the dielectric spacing was ruled out for in-chip failure, the in-chip *I-V* data was further analyzed to determine possible parameters responsible for the failure distribution. Based on simulations using a charge transport model [103], variations in material parameters such as the dielectric constant (κ), electron energy barrier into the dielectric conduction band (Φ_B), and initial defect density ($C_{trap,0}$) will result directly affect the leakage current. Therefore, if one of these parameters is the driving force for the failure distributions, there will be a direct correlation between the total injected charge ($Q_{inj} = \int I\, dt$) measured at a common voltage and the breakdown voltage for a group of in-chip samples. Figure 4.17 shows the results for this analysis. There is no correlation between Q_{inj} measured at 19.9 V (black circles) and the breakdown voltage for a group of samples on the same chip. κ, Φ_B, and $C_{trap,0}$ must therefore all be the same between these samples. This also further validates that dielectric spacing is uniform between in-chip samples.

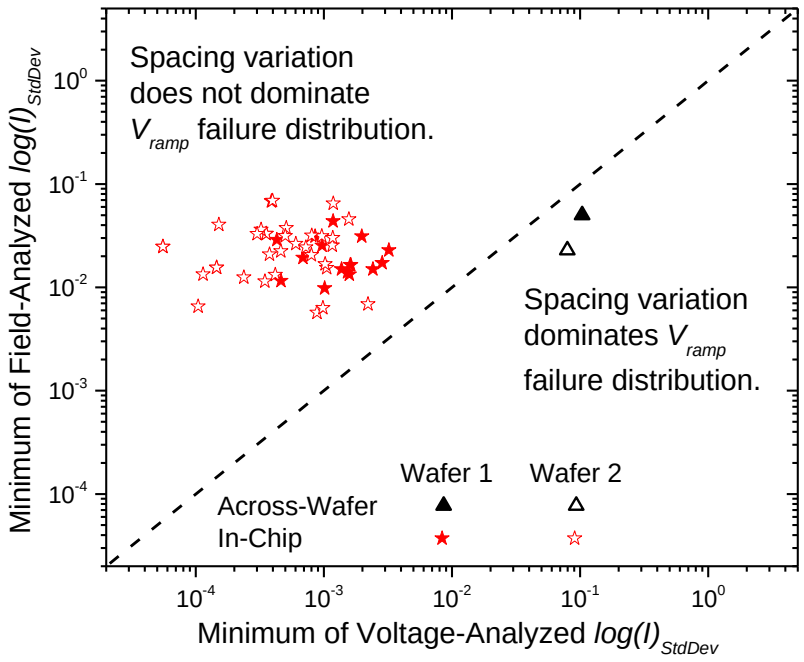

Figure 4.16. Comparison between minimum of $log(I)_{StdDev}$ values analyzed by voltage and electric field for all wafers and chips tested. Data below the dash line indicates spacing-dominated failure.

Instead, the samples' varying V_{BD} is driven by a parameter that has no connection to the electron conduction through the dielectric. As seen in Figure 4.17, there is a direct correlation between the charge-to-breakdown (Q_{BD}) and the breakdown voltage; samples that failed at a higher voltage endured larger electron fluences. One possible explanation can be argued based on percolation path theory for oxide dielectrics. A previous study on SiO_2 gate oxides reported that dielectric breakdown occurs when a critical defect density is reached and a conductive (percolation) path is formed at the weakest location in the dielectric [102]. This study found that charge-to-breakdown (Q_{BD}) variations between samples of uniform thickness were not due to process-induced defects, but rather the oxide degradation mechanism [102].

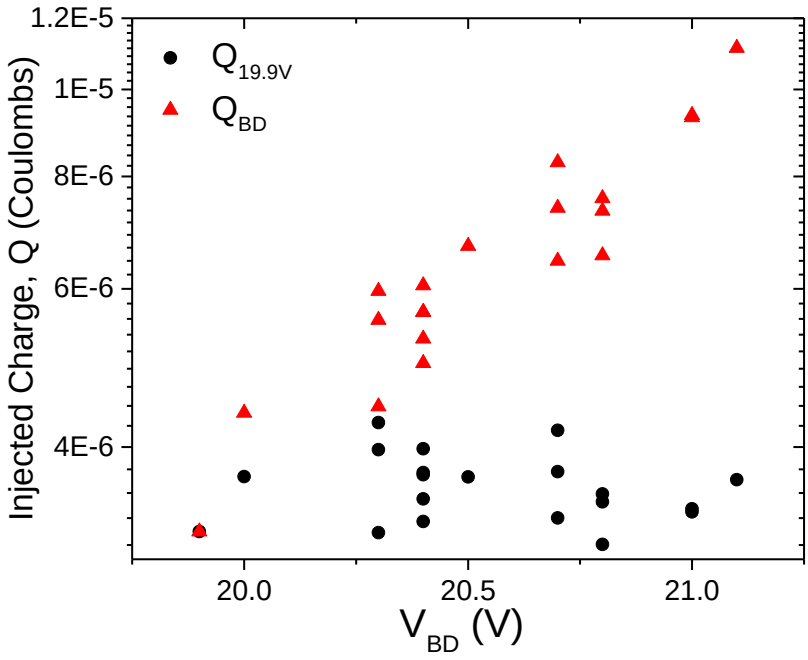

Figure 4.17. Injected charge, Q_i, measured at a common voltage of 19.9 V (black circles) and at the breakdown voltage (red triangles) as a function of the breakdown voltage for in-chip samples. There is no correlation between $Q_{19.9V}$ and the breakdown voltage.

This explanation can also apply to the in-chip failure results for low-κ SiCOH dielectrics. These materials are amorphous, and therefore small differences in composition between samples change their degradation, or rate of defect generation. Experimentally, this can be expressed as samples exhibiting different dielectric strength values (E_{BD}). In the charge transport model, the enthalpy for defect formation (ΔH) can explain this behavior. This parameter relates to the strength of the bonds that are broken in the dielectric, but does not affect the conduction or critical defect density for failure.

4.2.4.2 Spacing-Dependent Failure Prediction

The previous section showed each chip on a wafer has a unique spacing, which can be calculated directly from a voltage ramp test. These spacing values can be inputted directly into the charge transport model to re-produce TDDB failure distributions, in order to determine if the spacing-driven failure also extends to constant-voltage stress. The dielectric spacing for each chip was calculated from multiple voltage ramp tests

using $S_{chip}=V_{BD,63\%}/E_{BD}$ [27], [29]. $V_{BD,63\%}$ is the 63rd percentile breakdown voltage calculated for each chip using a Weibull distribution, also known as the Weibull scale parameter. E_{BD} is the breakdown strength of the dielectric and was determined to be 0.75 V/nm for the test structure and experimental conditions used in this work [29]. Figure 4.18 shows a wafer map with the dielectric spacing for approximately half the chips on the wafer. The spacing is normalized to the 63% Weibull value. Overall, the distribution is fairly tight between the wafers, indicating the spacing does not vary drastically across the wafer. The thinnest samples are located at the wafer edge. This is typically the case, as the line/via size (also called the critical dimension) and overlay are difficult to control far away from the wafer center, resulting in thinner minimum spacings.

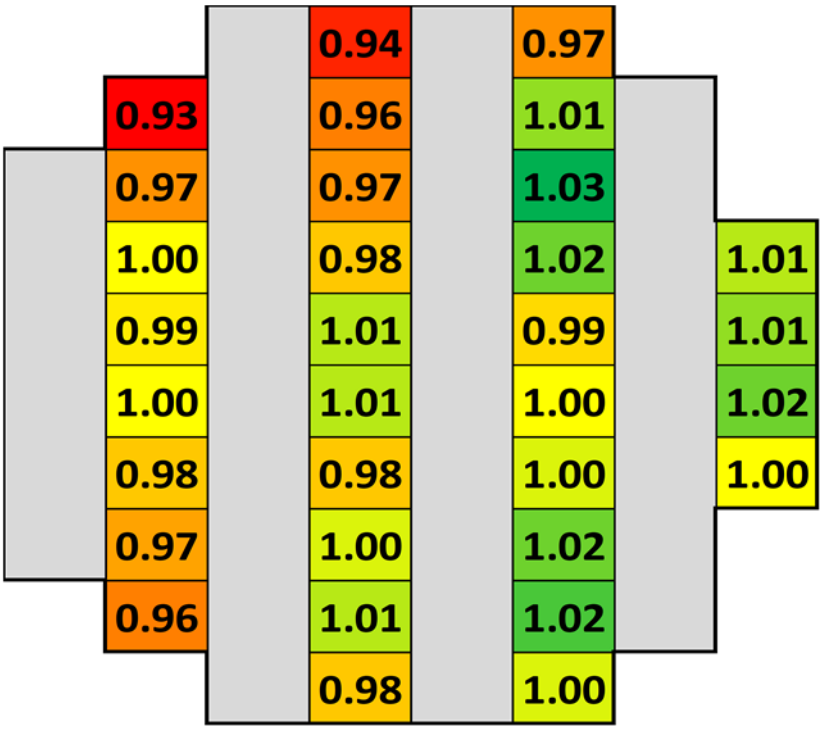

Figure 4.18. Wafer map showing the calculated dielectric spacing for half of the die on the wafer, normalized to the Weibull 63% value. The wafer map signature shows several edge die with the smallest spacing, but the overall distribution is fairly tight between the various die.

Two wafers were tested for model comparison, and the cumulative distribution function (CDF) of the calculated dielectric spacing for each wafer is shown in Figure 4.19. Each data set appears to follow a Weibull distribution, although a larger sample

size is necessary to gain statistical confidence in the distribution fit to the low-percentile, small spacing samples. Overall, the samples in Wafer 1 had higher V_{BD}, and therefore larger calculated spacing values, compared to Wafer 2. Based on the Weibull fit, the two data sets have a similar distribution shape (β~50). Based on these results, it is expected that Wafer 1 performs slightly better than Wafer 2 during TDDB tests.

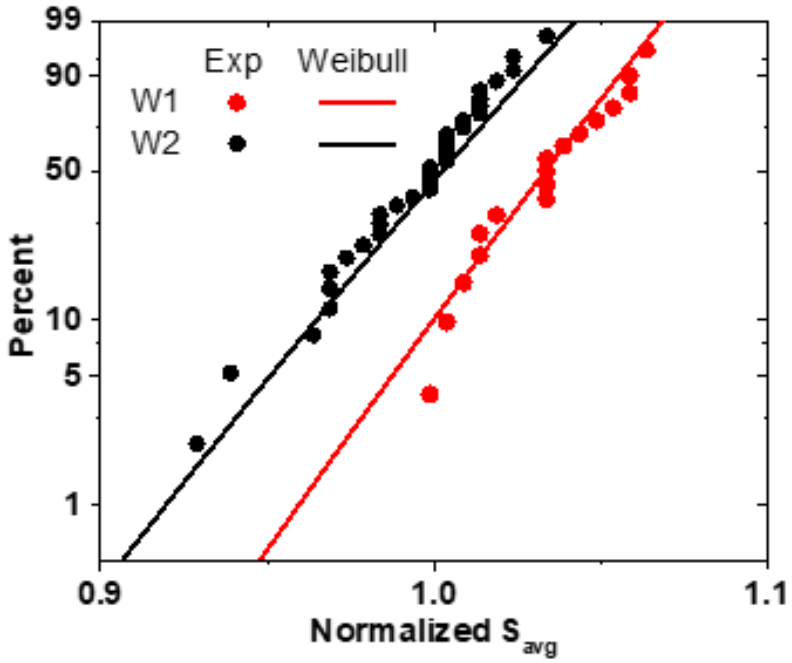

Figure 4.19. Spacing distribution profiles for two tested wafers. The dielectric spacing for each tested chip was calculated based on the breakdown data from voltage ramp tests. Both wafers were fitted to Weibull distributions (solid lines).

The same parameters calculated in Section 4.2.2 and listed in Table 4.1 were used here. All parameters were kept constant for each simulation, except for the applied voltage (V_{app}) and the dielectric spacing (s). Simulations were run for each experimental voltage, and for each dielectric spacing shown in Figure 4.19. This approach directly ties the V_{BD} voltage ramp results to the TDDB failure distributions. Figure 4.20 shows the Weibull plot experimental and simulation TDDB results for Wafer 1 (13 V to 16 V). Each symbol for the experimental results represents $t_{63\%}$ for each chip (based on 10 stressed samples per chip). Each symbol for the model results represents a simulation run for each calculated chip spacing from Figure 4.19.

The CT model provides an excellent prediction of the failure distributions for a voltage range of 13 V to 16 V. These initial results provide further validation that the spacing variation dominates both the V_{ramp} and TDDB failure distributions, and the minimum dielectric spacing for each chip can be calculated based on its V_{ramp} breakdown voltage results. There are two main advantages from predicting TDDB failure based solely on V_{ramp} tests. First, a voltage ramp test typically lasts less than a minute, compared to a TDDB test, which can range from minutes to days depending on the stress voltage. Thus, data and reliability projections can be collected much quicker than standard TDDB testing. Second, due to quicker test time, more V_{ramp} tests can be conducted overall compared to TDDB. A larger sample size means a smaller projection from the main population samples to the early failure rate limit, increasing the confidence in the projection. The number of chips on each wafer is limited, based on the wafer and chip sizes, but multiple wafers can be tested and combined to provide an overall reliability projection for the manufacturing line.

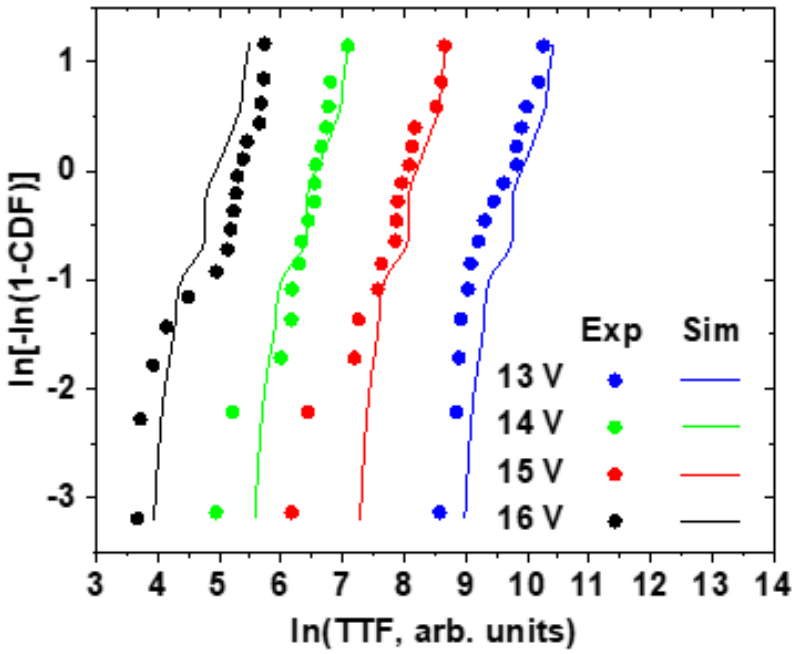

Figure 4.20. Experimental (circles) and simulation (solid lines) TDDB results on a Weibull plot for Wafer 1. The CT model predicts average failure times and overall failure distributions extremely well.

Figure 4.21 shows the Weibull plot experimental and simulation TDDB results for Wafer 2 (11 V to 15 V), tested at lower voltages. Again, the model is able to predict the failure times and failure distributions fairly accurately. The model predicts a slightly higher Weibull shape (β), but it can be seen from the large data set collected at 15 V that the model and experiment agree very well down to the early population failures. This data set provides validation that the model can be applied to multiple wafers, only needing to change the spacing parameter in order to provide failure distributions as a function of voltage.

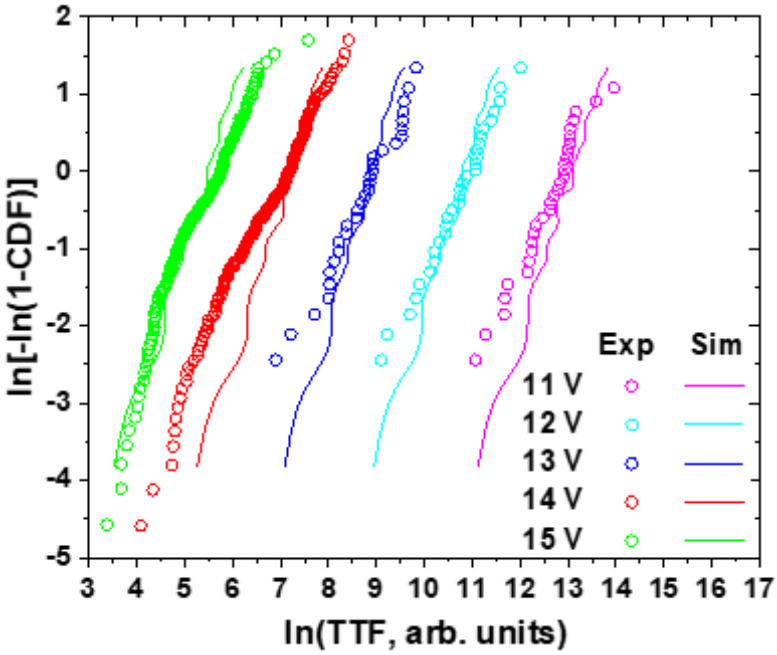

Figure 4.21. Lower voltage experimental (circles) and simulation (solid lines) TDDB results on a Weibull plot for Wafer 2. The model again shows a good fit to the experimental data, despite only inputting the spacing as a parameter.

4.3 Scaling Effects

The model has thus far shown useful in its ability to predict and explain experimental trends, and provide an inside look at the dielectric breakdown process. However, a critical need for reliability engineers is to understand and predict dielectric failure for future technology nodes, as the device dimensions continue to shrink. Here, the model is

applied to predict variability and dielectric strength trends as the dielectric spacing continues to decrease for newer generation devices.

4.3.1 Weibull Beta Trends

First, the CT model was used to predict variability trends in future technology. The model parameters and spacing distribution for Wafer 1 from Section 4.2.4.2 was used as a reference. The values for every calculated spacing were shifted a certain amount, such that the distribution shape was unaffected, but the average spacing decreased. This offers a very simple representation of how the dielectric thickness could vary across a wafer for future technology nodes if the same manufacturing processes are used. These altered spacing distributions were inputted into the model and simulated at constant voltages set to values such that the s_{avg} for each distribution were subjected to the same average nominal electric field (E_{avg}=0.5 V/nm). Each resulting failure distribution was then fitted to the Weibull function, and the Weibull shape parameter (β) was plotted as a function of normalized s_{avg}, as shown in Figure 4.22. The shaded error represents the standard error for the β calculation. A smaller β indicates decreased reliability, as the low percentile failures will occur at shorter failure times. The graph shows that as the average dielectric thickness decreases, β also decreases, following a linear relationship.

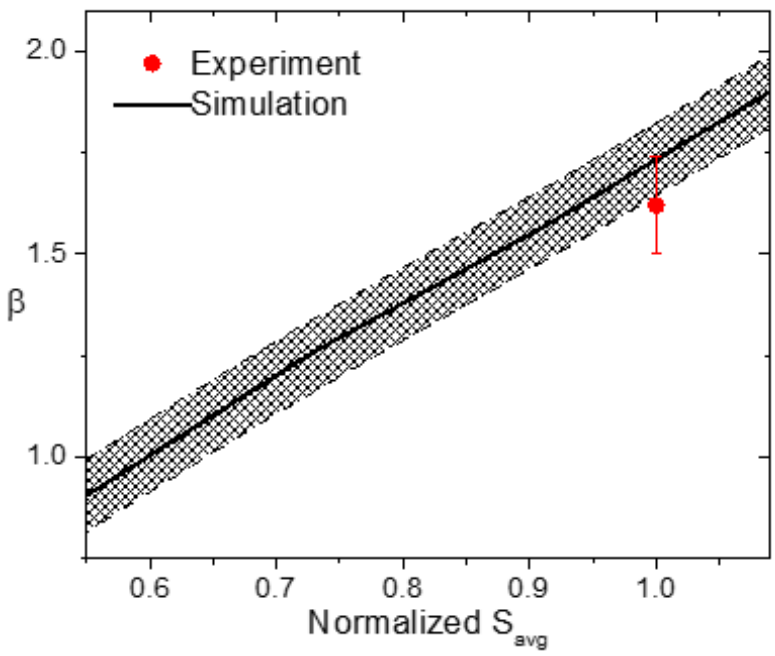

Figure 4.22. β predictions by the CT model for future nodes (decreasing (s_{avg}). The relationship between β and s_{avg} is based on continued use of current manufacturing technology.

Figure 4.22 only represents a simplified prediction of reliability trends based on current manufacturing processes. These trends could actually be worse in reality, as line-edge-roughness has been shown to become rougher as the line-to-line spacing is decreased [124]. However, manufacturing technology usually evolves to improve line definition with each emerging node in order to counteract this reliability degradation.

A limitation of this model's application to predict failure distributions is based on the assumption that the dielectric breakdown location will always occur at the minimum spacing. This assumption is valid for V_{ramp} tests and the high voltage ranges tested in this paper. However, as the voltage approaches the operating voltage, the breakdown is actually expected to occur in a median dielectric thickness location due to electric field enhancement of the pores [125]. In order to be able to replicate this, the model will need to be altered to a two-dimensional or a pseudo-1D model similar to [125], simulating the enhanced electric field around the pores. This will improve reliability projections, as the failure may not actually occur at the minimum dielectric spacing.

4.3.2 Dielectric Spacing Trends

The charge transport model can also be used to predict the effect of thickness on dielectric breakdown. Voltage ramp simulations were run for various dielectric thicknesses, and the dielectric strength for each thickness was calculated using $E_{BD} = V_{BD}/s$. Figure 4.23 shows that the dielectric strength increases as the dielectric thickness decreases. The model's thickness dependence originates from the Lorentz factor (L), which is approximately 1/3 for ultra-thin dielectrics (<2 nm), but approaches 1 for >20 nm insulators. The thickness-dependent Lorentz factor was introduced by McPherson [109], who shows a power law dependence between the thickness and dielectric strength, with a power law exponent n = 0.18 for SiO_2. Using the same equation from [109], low-κ SiCOH with κ = 2.7 will produce n = 0.13. A power law fit to the simulation results yields n = 0.10, which is close to, but slightly lower than, the theoretical prediction. This lower value is due to the electron temperature in the defect generation, which acts to slightly damp the effect of the dielectric thickness on the breakdown process.

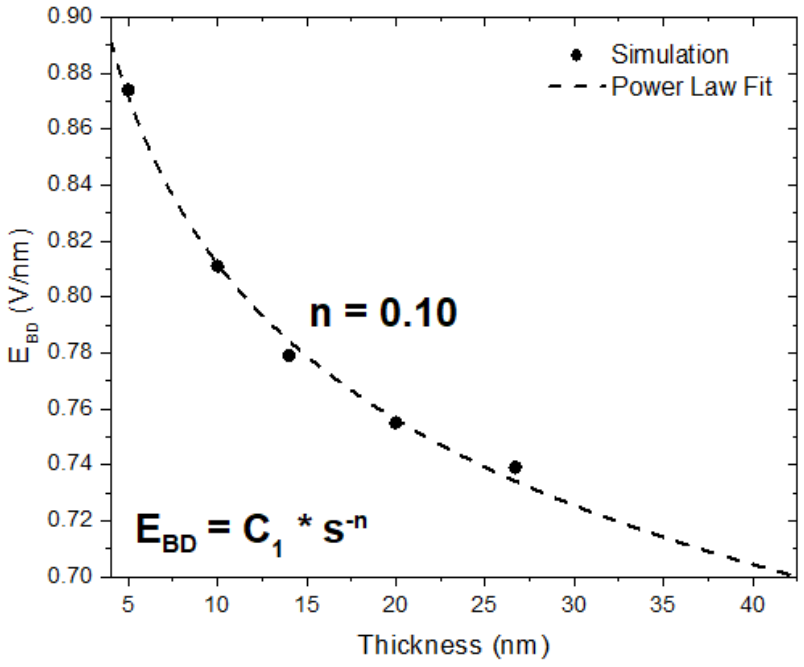

Figure 4.23. Model prediction of the dielectric strength as a function of minimum dielectric thickness. The dielectric strength increases with a power law dependence to the thickness, with n = 0.10 for low-κ SiCOH.

This trend also has important reliability implications, as it predicts thinner dielectric materials will fail at a longer time compared to a thicker dielectric material stressed under identical electric fields. To calculate the relative lifetime improvement, constant voltage stress simulations were run for samples with a thickness of 5 nm, 10 nm, and 20 nm. Figure 4.24 shows the simulation results, as well the fit for each simulation data to the $E^{1/2}$ model. Again, the choice of model is arbitrary, and is only used to predict lifetime at operating conditions for comparison between the simulations. The empirical lifetime model is necessary because the charge transport model has a lower limit based on the concentration of mobile electrons. The $E^{1/2}$ model parameters and lifetime prediction for each dielectric thickness simulation are shown in Table 4.3. The failure vs. field slope, defined as γ in the $E^{1/2}$ model, increases as the dielectric thickness decreases. From 20 nm to 5 nm, γ increases ~10%. The lifetime projection at 1 MV/cm, based on the $E^{1/2}$ model, improves by a 6x factor as the dielectric thickness thins by half (from 20 nm to 10 nm and from 10 nm to 5 nm). This will provide some margin for reliability in future technology nodes, although this will be counteracted by increasing variability. It should also be noted that these simulations were one-dimensional, and are therefore only valid for planar dielectric structures. For integrated structures, geometry effects such as enhanced electric fields near the electrodes may also cause reliability to degrade for future technology nodes.

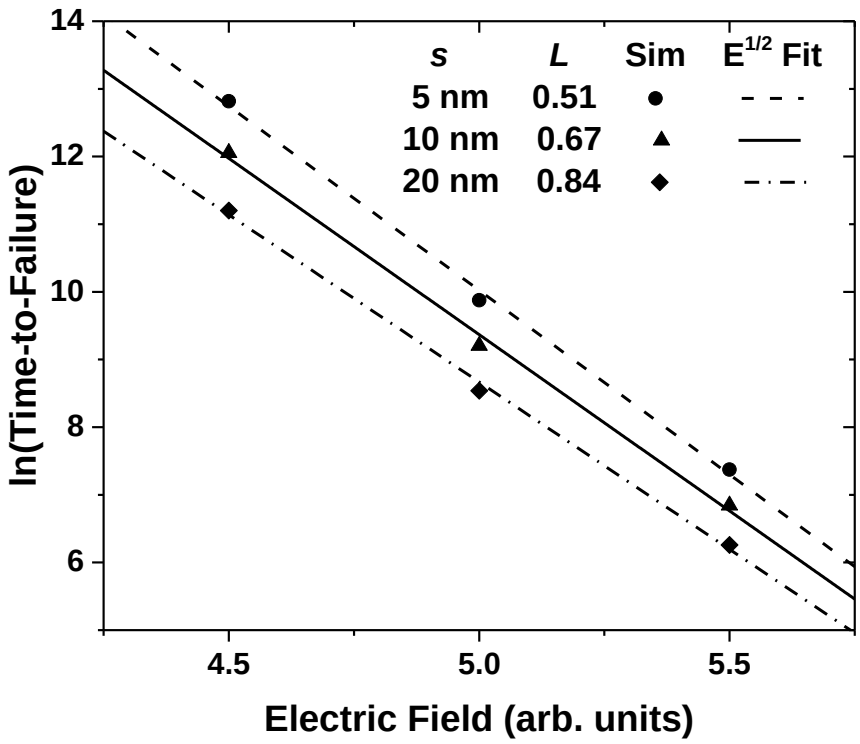

Figure 4.24. Simulations and corresponding fits using the $E^{1/2}$ model for low-κ SiCOH with 5 nm, 10 nm, and 20 nm thickness. Overall, the failure time and failure vs field slope increase as thickness decreases.

Table 4.3. Lifetime comparisons for TDDB simulations with different dielectric thicknesses. The failure vs. field slope and relative dielectric lifetime increase as dielectric thickness decreases.

***s* (nm)**	***L***	**$E^{1/2}$ Model Parameters**		**Relative LT**
		A	**γ**	**@ 1 MV/cm**
5	0.51	1.5×10^{16}	5.44	28
10	0.67	2.4×10^{15}	5.21	6
20	0.84	3.2×10^{14}	4.94	1

5. CONCLUSIONS AND FUTURE WORK

Dielectric breakdown is an immensely vast and complex topic, studied in great depth for almost 100 years to date. This work aims to replicate this phenomenon by grasping the most important aspects pertaining to the nature of dielectric failure. The charge transport model is more comprehensive than the vast majority of proposed dielectric failure models. Yet, due to the intricate nature of dielectric failure and the diverse industrial applications for insulators, this model is, and always will be, a work in progress. This chapter details the main findings and advantages of the charge transport model, and also proposes several directions toward which the model can be expanded and further developed.

If you think in terms of a year, plant a seed;
if in terms of ten years, plant trees;
if in terms of 100 years, teach the people."
-Confucius

5.1 Conclusions

The charge transport model is presented in this work in two stages: an initial model, followed by a refined version. The initial proposed model provides a solid foundation towards understanding dielectric breakdown, and is able to replicate leakage and failure data for multiple dielectric materials. The refined model builds upon this initial offering by re-evaluating some of the early model's concepts and incorporating newly proposed failure theories.

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5.1.1 Initial Results of the Charge Transport Model

The first proposal of the charge transport model, presented in Chapter 3, was initially applied to predict the lifetime of dielectric materials used in integrated circuits. The model is based on electron transport through the dielectric and donor-type defect formation. Breakdown occurs when the defects reach a critical density, causing the emptying of traps due to electron tunneling. This leaves behind positively charged traps and catalyzes a positive feedback failure mechanism.

The charge transport model is able to predict TTF versus field accurately for multiple low-field and high-field low-κ SiCOH and high-κ SiN experiments. Extrapolations to even lower fields indicate that the use of a single reliability model might not be an accurate method to predict lifetime. The charge transport model can therefore be used to improve understanding for device lifetime prediction based on parameters that depend on the physical properties of the dielectric material and in theory, could be related to the composition and structure of the material. Comparison of model parameters between SiCOH and SiN shows silicon nitride films have improved reliability due to their higher dielectric constant and deeper defect energy levels.

Three potential advantages of the charge transport model over typical reliability models for lifetime predictions were demonstrated in Chapter 3:

1. The charge transport model is able to replicate I-V and I-t trends, including the magnitude of the early leakage current, the current decay and the abrupt increase in current at failure. Overall, the breakdown mechanism in the charge transport model is both current-driven and field-driven.
2. The charge transport model relies on three material parameters that are determined from experimental data. None of these parameters are altered to fit the slope of the TTF versus field curves. The only parameter that is adjusted to obtain the correct TTF is the enthalpy of activation (ΔH), which can be determined using a single experimental data point.
3. The parameters used in the charge transport model are all consistent with theoretical or experimental values reported for dielectric materials.

However, the charge transport model in its initial form also suffers from several limitations. The model was found to over-predict the temperature dependence for dielectric failure. In addition, none of the equations provided any direct contribution of the dielectric spacing to the failure, except tied to the electric field.

5.1.2 Results for the Refined Charge Transport Model

These model limitations were addressed through several revisions to the equation set. In order to reduce the temperature dependence for dielectric failure, the electron temperature was revised based on an electron equilibrium equation dependent on the electric field, without any decaying due to the buildup of defects. The defect generation equation was also changed from a $F^{1/2}$ to a linear-F dependence, consistent with the thermo-chemical model for breaking bonds, assumed to be Si-H for the silicon-based dielectrics discussed in this work. A thickness dependence was also added into the polarized field equation, based on a newly proposed theory for the thermo-chemical model for planar dielectrics.

The new set of equations, termed the refined charge transport model, were also re-arranged into dimensionless form to assess the transport, kinetics, and failure trends, as described by the model. Analysis of the Péclet number found the electron transport to be convection-driven, and the Damköhler number for the defect generation rate found the reaction kinetics to be very slow. Analysis of the local electric field yielded several interesting trends based on the dielectric thickness and nominal electric field. Thinner dielectrics yield ψ-ξ slopes closer to zero compared to thicker dielectrics, due to a lower Q value in the Poisson's equation. This results in a lower ψ at the cathode for thinner dielectrics compared to thicker dielectrics when a net negative charge exists in the dielectric, but a higher ψ for a net positive charge (which occurs at lower electric fields).

The model shows a very clear correlation between the leakage current and dielectric failure for low-κ SiCOH. A field-dependent activation energy can be attributed to the energy barrier for electron injection into the dielectric, which is the boundary condition dictating the electrons' conduction. Dielectric failure activation energies up to 1 eV are predicted by the model at operating conditions of 1 MV/cm, which can provide a drastic lifetime boost for chips operating at lower temperatures. The model also shows

that planar dielectrics show improved strength as their thickness decreases. This may not be the case for integrated structures which suffer from enhanced electric fields due to geometrical effects. The model also was shown to predict dielectric failure distributions based solely on changing the dielectric spacing parameter. The spacing was estimated for each die across multiple wafers based on V_{ramp} tests. As the dielectric thickness continues to decrease for thinner wafers, variability will worsen, and overall reliability will degrade.

5.2 Future Work

The charge transport model has proven a useful tool to describe the breakdown process of dielectric failure, and predict breakdown trends for current and future technology nodes for integrated circuits. There are many new directions in which the model can be further developed to improve its applicability to the semiconductor industry. This section discusses the most intriguing topics for which the charge transport model can be modified or applied to continue to improve the understanding of dielectric breakdown, especially as it pertains to integrated circuits.

5.2.1 Detailed Defect Study

There are several model parameters relating to the defects in the dielectric. The initial defect density ($C_{trap,0}$) defines the amount of positive charges in the dielectric, and also determines the initial scattering length for defects (λ_{trap}). The defect density required to initiate the breakdown process was shown to depend on the energy level of the defects (Φ_{trap}). In addition, the defect generation rate is strongly controlled by the enthalpy of activation (ΔH) and the effective molecular dipole moment (α). Clearly, the type of defects initially present and generated throughout the stress are extremely important to the failure trends and overall reliability of the dielectric material. Presently, the best approach to estimate these parameters is through previously reported measurements/calculations, and/or assumptions based on the weakest known bonds in the dielectric. This approach has proven adequate, but also creates a level of uncertainty in each of the parameters. This uncertainty can either cause model deviations from the experimental data, or get carried forward into the adjustable parameters. An alternate

approach is to directly measure these parameters on dielectric films, and then electrically stress the same films to extract information about the electron conduction and failure. Electron spin resonance (ESR) and electrically detected magnetic resonance (EDMR) have been demonstrated as effective techniques to measure the density of defects and their corresponding energy levels.

The proposed study is to collaborate with Dr. Lenahan's group at Penn State, an established lab well-known for employing ESR and EDMR techniques [32], [74] to measure dielectric defect properties. The purpose is to study dielectric films with different defect types. For this, silicon nitride is the ideal film to study. The ratio of silicon to nitride can be controlled by changing the ratios of the pre-cursor gases and the deposition pressure. Previous studies have found that silicon dangling bonds typically dominate in silicon-rich alloys, while nitrogen dangling bonds are present in nitrogen-rich alloys [98]. The defect types can also depend on the processing conditions, such as high-temperature anneal [126]. For each film, $C_{trap,0}$ and Φ_{trap} will be directly measured using ESR and EDMR, providing the crucial information about the types of defects present in the dielectric. From this information, ΔH and α will be inferred. The remaining model parameter estimation approach will remain the same; extract from literature reports, or determine from the electrical data. This study is expected to yield two main results. First, the direct measurements of the dielectric films will remove parameter uncertainties, and improve the confidence in the model if able to replicate the electrical data. In addition, the effect of the defects on electrical conduction and reliability can be more closely tied to the defect parameters, based on the results of the experiments and corresponding model fits.

5.2.2 Metal Ion Failure

The charge transport model presented in this work has dealt exclusively with intrinsic breakdown mechanisms, i.e., dielectric failure as it relates solely to electronic conduction and subsequent defect generation. However, extrinsic failure modes have also been reported, especially for low-κ SiCOH films. One of the most prominent and threatening extrinsic breakdown mechanisms relates to metal ion contamination. The introduction of copper wires, in conjunction with porous SiCOH films, created an

unstable metal-dielectric interface. Copper atoms are readily oxidized by the oxygen atoms in the dielectric, and the porous network of the insulator allows these copper ions to move easily through the dielectric. These copper ions can increase the local field at the cathode and form a conductive pathway for failure to occur. As a result, copper-catalyzed failure has been studied extensively [21], [22], [30], [35], [127].

However, there is still some dispute about the effect of metal ion failure on dielectric failure trends. Planar dielectric studies employing variable voltage ramp tests and variable frequency bipolar tests have shown that copper migration affects the dielectric failure at slow ramp rates and low frequencies, when the copper has sufficient time to move across the dielectric [21], [22], [30]. For tests with short failure times, such as a voltage ramp with a fast ramp rate or high-field TDDB, copper is not able to migrate across the dielectric and the failure mode is intrinsic-driven. Thus, these studies found copper-driven breakdown followed a E^2 dependence [128]. On the other hand, the $E^{1/2}$ model is based on Poole-Frenkel conduction through copper-based defects [35]. Another study reported copper-catalyzed failure was best represented by the $1/E$ model [127], where copper reduces the failure times at high electric fields, but its effect diminishes as the field decreases.

In the current technology nodes, the assumption of intrinsic-driven failure is valid, as the process is optimized to eliminate or significantly reduce the effect of copper ions through the introduction of Ta/TaN barrier materials. However, as the interconnect dimensions continue to shrink, these barriers must also scale accordingly. Thus, the importance of metal-catalyzed failure will re-emerge as a potential breakdown mechanism in the future nodes. Metals such as Ru, Co, and W are also being explored to replace copper in the interconnect, both for reliability and resistance purposes. Thus, it will be crucial to understand the solubility and diffusivity of each of these metals to fully explain how metal-catalyzed failure affects dielectric reliability and to provide direction on which metals are viable for future nodes. The charge transport model represents the optimum platform for this type of study. The equations for intrinsic failure will be combined with previously developed equations for metal ion transport [13]. Both planar dielectrics and integrated structures will be studied in order to compare sample configuration on the failure process.

5.2.3 2-D Simulations

The model, in its current one-dimensional form, can be used to generate information about the breakdown nature of the material based on a limited amount of experimental *I-V* or *I-t* data. The 1-D model can also be used to explain and predict dielectric trends, compare dielectric materials, and measure the effect of process variability such as dielectric thickness or compositional variations. However, transitioning the model from 1-D to 2-D will greatly improve its accuracy and expand its applicability.

A two-dimensional implementation will enable the charge transport model to explore the effects of geometry on conduction and overall reliability. In the present, 1-D form of the equations, geometrical effects are all lumped in to the parameters, mainly A_{eff} (or P_{eff}) and η. These two adjustable parameters at least partially represent conversions from a 1-D to 2-D platform. However, the parameters are limited to a generalization of the conduction and defect generation. Expansion into 2-D will allow the equations to separate out the effects of non-uniformities in the sample. These non-uniformities include: enhanced field and conduction at the SiCOH/SiCN:H capping layer due to the sidewall angle of the metal trenches and discontinuity in the dielectric constant, variation in the dielectric thickness across the electrodes due to line edge roughness and via placement, and small perturbations in the chemical composition that may lead to drastically different defect generation rates.

Dielectric breakdown dictated by multiple variable randomness can lead to deviations from currently used statistical models. A clustering model was introduced to properly calculate failure distributions (instead of Weibull distributions) and area scaling (instead of Poisson area scaling), based on non-uniform defect distributions in the dielectric [55], [129]. While the Weibull distribution is only valid for a single random variable, the authors showed the clustering model is more applicable for dielectric failure in integrated circuits due to the competition between defect non-uniformity and thickness variations in the dielectric [130]. 2-D simulations using the charge transport model can provide a useful tool to examine the effect of these competing variables. Initial defect densities can be inputted into the model using a gamma distribution function, similar to the clustering model. This density variation can then be combined

with various thickness variation effects, such as line edge roughness or line overlay, to examine the resulting failure distributions that might occur in-die or across-wafer, respectively. There are several claims by the clustering model for which the charge transport model can provide some clarity. First, the clustering model claims that at early failure percentiles, the failure distributions converge towards the Weibull distributions, due to low defect densities that prevent any defect "clustering" [129]. However, this seems counter-intuitive because the earliest failing samples should be dictated by the highest defect densities, for which clustering would be extremely important. Second, the clustering model statistics show that as the overall failure variability increases (lower β), the overall model also converges to a Weibull distribution. This could be an indication that spacing variation starts to dominate over defect density, reverting back to a single random variable case that can be appropriately modeled using a Weibull distribution. The charge transport model can be applied here as well, changing the effects of the spacing variation and defect non-uniformity to model the resulting failure distributions.

A 2-D model will also be useful to model the effects of an air gap in the dielectric between two metal lines. Air gaps are implemented into integrated circuits to improve the RC signal delay [131], but are difficult to manufacture and their effect on reliability is not well understood. In the 2-D model, an air gap can be easily implemented between two metal lines in order to map the gap's effect on conduction and overall failure path.

5.2.4 Final Thoughts

The topics discussed above (detailed defect study, metal-catalyzed failure, and 2-D simulations) represent just three ways the model can be applied or expanded right now to improve its functionality and relevance to the integrated circuit community. There are many other uses or improvements for the model that are either apparent now or will become so as new dielectric breakdown theories are presented and different failure mechanisms emerge during the continued evolution of integrated circuits. New conduction mechanisms should be considered for films approaching 5 nm and below. It was also shown in Chapter 4 that the model may be missing a conduction mechanism at the highest applied fields, which could be tunneling or some other type of conduction.

Identifying and applying this additional conduction mechanism could be important to explain high-voltage TDDB behavior, which has serious implications for reliability engineers using statistical approaches to extrapolate to operating conditions.

The emergence of big data also represents an opportunity for the model presented in this work. Companies that fabricate large mass quantities of semiconductor wafers, such as GLOBALFOUNDRIES, also produce a large amount of data from these wafers. If this data is not completely and properly analyzed, the resulting inefficiencies cause decreased productivity. In terms of dielectric failure data, a collaboration between GLOBALFOUNDRIES and RPI can improve overall efficiency, tying together the failure data to the model theory in order to provide a complete and detailed picture of the dielectric breakdown process.

BIBLIOGRAPHY

[1] A. V. Gurevich and K. P. Zybin, "Runaway breakdown and the mysteries of lightning," *Phys. Today*, vol. 58, no. 5, pp. 37–43, May 2005.

[2] K. Yoshino, "Dependence of dielectric breakdown of liquids on molecular Structure," *IEEE Trans. Electr. Insul.*, vol. EI-15, no. 3, pp. 186–200, Jun. 1980.

[3] A. von Hippel, "Electric breakdown of solid and liquid Insulators," *J. Appl. Phys.*, vol. 8, no. 12, pp. 815–832, Dec. 1937.

[4] C. Zener, "A theory of the electrical breakdown of solid dielectrics," *Proc. R. Soc. Lond. Ser. Contain. Pap. Math. Phys. Character*, vol. 145, no. 855, pp. 523–529, Jul. 1934.

[5] H. Fröhlich, "Theory of electrical breakdown in ionic crystals," *Proc. R. Soc. Lond. Ser. Math. Phys. Sci.*, vol. 160, no. 901, pp. 230–241, May 1937.

[6] A. von Hippel, "Electronic conduction in insulating crystals under very high field strength," *Phys. Rev.*, vol. 54, no. 12, pp. 1096–1102, Dec. 1938.

[7] A. von Hippel, "Electric breakdown of solid dielectrics," *Trans. Faraday Soc.*, vol. 42, pp. A078–A087, Jan. 1946.

[8] H. Fröhlich, "Energy distribution and stability of electrons in electric fields," *Proc. R. Soc. Lond. A*, vol. 188, no. 1015, pp. 532–541, Feb. 1947.

[9] R. R. Schaller, "Moore's law: past, present and future," *IEEE Spectr.*, vol. 34, no. 6, pp. 52–59, Jun. 1997.

[10] M. Shur, *Introduction to Electronic Devices*. New York, NY, USA: Wiley, 1996.

[11] J. S. Kilby, "Invention of the integrated circuit," *IEEE Trans. Electron Devices*, vol. 23, no. 7, pp. 648–654, Jul. 1976.

[12] M. Ohring, *Reliability and Failure of Electronic Materials and Devices*, 2nd ed. London, England: Elsevier, 2015.

[13] J. P. Borja, T.-M. Lu, and J. Plawsky, *Dielectric Breakdown in Gigascale Electronics*. Cham, Switzerland: Springer, 2016.

[14] G. E. Moore, "Cramming more components onto integrated circuits", vol. 38, no. 8, pp. 114–116, Sep. 2006.

[15] B. J. Lin, "Making lithography work for the 7-nm node and beyond in overlay accuracy, resolution, defect, and cost," *Microelectron. Eng.*, vol. 143, pp. 91–101, Aug. 2015.

[16] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," *IEEE Trans. Electron Devices*, vol. 31, no. 4, pp. 452–462, Apr. 1984.

[17] J. Srinivasan, S. V. Adve, P. Bose, and J. A. Rivers, "The impact of technology scaling on lifetime reliability," in *Proc. 2004 Int. Conf. Dependable Systems and Networks*, 2004, pp. 177–186.

[18] G. S. Haase, E. T. Ogawa, and J. W. McPherson, "Breakdown characteristics of interconnect dielectrics," in *Proc. 43rd Annu. Rel. Phys. Symp.*, 2005, pp. 466–473.

[19] L. Zhao *et al.*, "Direct observation of the 1/E dependence of time dependent dielectric breakdown in the presence of copper," *Appl. Phys. Lett.*, vol. 98, no. 3, Jan. 2011, Art. no. 032107.

[20] J. M. Atkin, T. M. Shaw, E. Liniger, R. B. Laibowitz, and T. F. Heinz, “The effect of voltage bias stress on temperature-dependent conduction properties of low-k dielectrics,” in *Proc. IEEE Int. Rel. Phys. Symp.*, 2012, pp. BD.1.1-BD.1.6.

[21] R. S. Achanta, J. L. Plawsky, and W. N. Gill, “A time dependent dielectric breakdown model for field accelerated low-k breakdown due to copper ions,” *Appl. Phys. Lett.*, vol. 91, no. 23, Dec. 2007, Art. no. 234106.

[22] J. Borja, J. L. Plawsky, T.-M. Lu, and W. N. Gill, “On the dynamics of Cu ions injection into low-k nanoporous materials under oscillating applied fields,” *J. Appl. Phys.*, vol. 113, no. 3, Jan. 2013, Art. no. 034104.

[23] J. Michelon and R. J. O. M. Hoofman, “Moisture influence on porous low-k reliability,” *IEEE Trans. Device Mater. Reliab.*, vol. 6, no. 2, pp. 169–174, Jun. 2006.

[24] Y. Li *et al.*, “Influence of absorbed water components on SiOCH low-k reliability,” *J. Appl. Phys.*, vol. 104, no. 3, Aug. 2008, Art. no. 034113.

[25] M. Stucchi, P. J. Roussel, Z. Tőkei, S. Demuynck, and G. Groeseneken, “A comprehensive LER-aware TDDB lifetime model for advanced Cu interconnects,” *IEEE Trans. Device Mater. Reliab.*, vol. 11, no. 2, pp. 278–289, Jun. 2011.

[26] K. Croes, I. Ciofi, D. Kocaay, Z. Tőkei, and J. Bömmels, “Effect of line-overlay and via-misalignment on dielectric reliability for different patterning schemes,” in *Proc. IEEE Int. Rel. Phys. Symp.*, 2014, p. BD.5.1-BD.5.4.

[27] F. Chen *et al.*, “New electrical testing structures and analysis method for MOL and BEOL process diagnostics and TDDB reliability assessment,” in *Proc. IEEE Int. Rel. Phys. Symp.*, 2013, pp. PI.1.1-PI.1.5.

[28] F. Xia *et al.*, “Characterization and challenge of TDDB reliability in Cu/low k dielectric interconnect,” in *Proc. IEEE Int. Rel. Phys. Symp.*, 2011, pp. 2C.1.1-2C.1.4.

[29] K. B. Yeap, F. Chen, H. W. Yao, T. Shen, S. F. Yap, and P. Justison, “A realistic method for time-dependent dielectric breakdown reliability analysis for advanced technology node,” *IEEE Trans. Electron Devices*, vol. 63, no. 2, pp. 755–759, Jan. 2016.

[30] J. L. Plawsky, J. Borja, B. Williams, M. J. Riley, and W. N. Gill, “Variable ramp rate breakdown experiments and the role of metal injection in low-k dielectrics,” *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4354–4360, Dec. 2011.

[31] L. Zhao, Z. Tőkei, G. G. Gischia, M. Pantouvaki, K. Croes, and G. Beyer, “A novel test structure to study intrinsic reliability of barrier/low-k,” in *Proc. IEEE Int. Rel. Phys. Symp.*, 2009, pp. 848–850.

[32] M. J. Mutch *et al.*, “Band diagram for low-k/Cu interconnects: The starting point for understanding back-end-of-line (BEOL) electrical reliability,” *Microelectron. Reliab.*, vol. 63, pp. 201–213, May 2016.

[33] F.-C. Chiu, “A review on conduction mechanisms in dielectric films,” *Adv. Mater. Sci. Eng.*, Feb. 2014. doi: 10.1155/2014/578168 [Online].

[34] F. Chen *et al.*, “A comprehensive study of low-k SiCOH TDDB phenomena and its reliability lifetime model development,” in *Proc. IEEE Int. Rel. Phys. Symp.*, 2006, pp. 46–53.

[35] N. Suzumura *et al.*, "A new TDDB degradation model based on Cu ion drift in Cu interconnect dielectrics," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2006, pp. 484–489.
[36] D. L. Crook, "Method of determining reliability screens for time dependent dielectric breakdown," in *Proc. 17th Annu. Rel. Phys. Symp.*, 1979, pp. 1–7.
[37] E. S. Anolick and G. R. Nelson, "Low field time dependent dielectric integrity," in *Proc. 17th Annu. Rel. Phys. Symp.*, 1979, pp. 8–12.
[38] A. Berman, "Time-zero dielectric reliability test by a ramp method," in *Proc. 19th Annu. Rel. Phys. Symp.*, 1981, pp. 204–209.
[39] J. W. McPherson and H. C. Mogul, "Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO_2 thin films," *J. Appl. Phys.*, vol. 84, pp. 1513–1523, Aug. 1998.
[40] I. C. Chen, S. Holland, and C. Hut, "A quantitative physical model for time-dependent breakdown in SiO_2," in *Proc. 23rd Annu. Rel. Phys. Symp.*, 1985, pp. 24–31.
[41] K. F. Schuegraf and C. Hu, "Hole injection oxide breakdown model for very low voltage lifetime extrapolation," in *Proc. 31st Annu. Rel. Phys. Symp.*, 1993, pp. 7–12.
[42] J. Sune and E. Wu, "A new quantitative hydrogen-based model for ultra-thin oxide breakdown," in *Symp. VLSI Tech. Dig. Tech. Papers*, 2001, pp. 97–98.
[43] K.-H. Allers, "Prediction of dielectric reliability from I–V characteristics: Poole–Frenkel conduction mechanism leading to $\sqrt{E}$ model for silicon nitride MIM capacitor," *Microelectron. Reliab.*, vol. 44, no. 3, pp. 411–423, Mar. 2004.
[44] J. R. Lloyd, E. Liniger, and T. M. Shaw, "Simple model for time-dependent dielectric breakdown in inter- and intralevel low-k dielectrics," *J. Appl. Phys.*, vol. 98, no. 8, Oct. 2005, Art. no. 084109.
[45] J. R. Lloyd, C. E. Murray, S. Ponoth, S. Cohen, and E. Liniger, "The effect of Cu diffusion on the TDDB behavior in a low-k interlevel dielectrics," *Microelectron. Reliab.*, vol. 46, no. 9, pp. 1643–1647, Sep. 2006.
[46] J. R. Lloyd, "On the physical interpretation of the impact damage model in TDDB of low-k dielectrics," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2010, pp. 943–946.
[47] E. Chery, X. Federspiel, D. Roy, F. Volpi, and J.-M. Chaix, "Identification of the ($\sqrt{E}$ + 1/E)-dependence of porous low-k time dependent dielectric breakdown using over one year long package level tests," *Microelectron. Eng.*, vol. 109, pp. 90–93, Sep. 2013.
[48] G. S. Haase, "A model for electric degradation of interconnect low-k dielectrics in microelectronic integrated circuits," *J. Appl. Phys.*, vol. 105, no. 4, Feb. 2009, Art. no. 044908.
[49] R. Moazzami, J. C. Lee, and C. Hu, "Temperature acceleration of time-dependent dielectric breakdown," *IEEE Trans. Electron Devices*, vol. 36, no. 11, pp. 2462–2465, Nov. 1989.
[50] M. Kimura, "Field and temperature acceleration model for time-dependent dielectric breakdown," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 220–229, Jan. 1999.
[51] N. Suzumura *et al.*, "Electric-field and temperature dependencies of TDDB degradation in Cu/Low-k damascene structures," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2008, pp. 138–143.

[52] F. Chen, M. Shinosky, J. Aitken, C. C. Yang, and D. Edelstein, "Temperature and field interrelation study of low-k TDDB for Cu interconnects with and without liner - New insights to the roles of Cu for a competing breakdown process," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2013, pp. 2F.2.1-2F.2.7.

[53] M. R. Baklanov, C. Adelmann, L. Zhao, and S. D. Gendt, "Advanced interconnects: materials, processing, and reliability," *ECS J. Solid State Sci. Technol.*, vol. 4, no. 1, pp. Y1–Y4, Jan. 2015.

[54] F. Chen *et al.*, "Breakdown data generation and in-die deconvolution methodology to address BEOL and MOL dielectric breakdown challenges," *Microelectron. Reliab.*, vol. 55, no. 12, pp. 2727–2747, Dec. 2015.

[55] E. Wu, B. Li, J. H. Stathis, R. Achanta, R. Filippi, and P. McLaughlin, "A time-dependent clustering model for non-uniform dielectric breakdown," in *Proc. IEEE Int. Electron Dev. Meeting*, 2013, pp. 15.3.1-15.3.4.

[56] R. S. Achanta, E. Wu, B. Li, and P. McLaughlin, "Analysis of applying time-dependent clustering model to BEOL TDDB," in *Proc. IEEE Int. Interconnect Tech. Conf.*, 2014, pp. 219–222.

[57] G. S. Canright and G. D. Mahan, "Time-dependent theory of hot electrons using the discrete Boltzmann equation," *Phys. Rev. B*, vol. 36, no. 2, pp. 1025–1031, Jul. 1987.

[58] G. D. Mahan, "Hot electrons in one dimension," *J. Appl. Phys.*, vol. 58, no. 6, pp. 2242–2251, Sep. 1985.

[59] S. Lombardo, J. H. Stathis, and B. P. Linder, "Breakdown transients in ultrathin gate oxides: transition in the degradation rate," *Phys. Rev. Lett.*, vol. 90, no. 16, Apr. 2003, Art. no. 167601.

[60] B. Ricco, M. Y. Azbel, and M. H. Brodsky, "Novel mechanism for tunneling and breakdown of thin SiO_2 films," *Phys. Rev. Lett.*, vol. 51, no. 19, pp. 1795–1798, Nov. 1983.

[61] B. J. Tang *et al.*, "As-grown donor-like traps in low-k dielectrics and their impact on intrinsic TDDB reliability," *Microelectron. Reliab.*, vol. 54, no. 9, pp. 1675–1679, Sep. 2014.

[62] C. Wu *et al.*, "Towards understanding intrinsic degradation and breakdown mechanisms in SiOCH low-k dielectrics," *J. Appl. Phys.*, vol. 117, no. 6, Feb. 2015, Art. no. 064101.

[63] M. Lundstrom, *Fundamentals of Carrier Transport*. Cambridge, England: Cambridge University Press, 2009.

[64] E. Kasper and D. J. Paul, *Silicon Quantum Integrated Circuits*. Berlin, Germany: Springer, 2005.

[65] G. G. Gischia, K. Croes, G. Groeseneken, Z. Tőkei, V. Afanas'ev, and L. Zhao, "Study of leakage mechanism and trap density in porous low-k materials," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2010, pp. 549–555.

[66] J. W. McPherson, "Time dependent dielectric breakdown physics – models revisited," *Microelectron. Reliab.*, vol. 52, no. 9, pp. 1753–1760, Sep. 2012.

[67] M. V. Fischetti, "Monte Carlo solution to the problem of high-field electron heating in SiO_2," *Phys. Rev. Lett.*, vol. 53, no. 18, pp. 1755–1758, Oct. 1984.

[68] R. H. Perry, D. W. Green, and J. O. Maloney, *Perry's Chemical Engineers' Handbook*, 6^{th} ed. New York, NY, USA: McGraw-Hill, 1984.

[69] J. Scarpulla, D. C. Eng, S. R. Olson, and C. S. Wu, "A TDDB model of Si_3N_4-based capacitors in GaAs MMICs," in *Proc. 31st Annu. Rel. Phys. Symp.*, 1999, pp. 128–137.
[70] A. Grill, S. M. Gates, T. E. Ryan, S. V. Nguyen, and D. Priyadarshini, "Progress in the development and understanding of advanced low k and ultralow k dielectrics for very large-scale integrated interconnects — state of the art," *Appl. Phys. Rev.*, vol. 1, no. 1, Mar. 2014, Art. no. 011306.
[71] F. Chen *et al.*, "The effect of metal area and line spacing on TDDB characteristics of 45nm low-k SiCOH dielectrics," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2007, pp. 382–389.
[72] K. Croes *et al.*, "Low field TDDB of BEOL interconnects using >40 months of data," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2013, pp. 2F.4.1-2F.4.8.
[73] A. Grill and D. A. Neumayer, "Structure of low dielectric constant to extreme low dielectric constant SiCOH films: Fourier transform infrared spectroscopy characterization," *J. Appl. Phys.*, vol. 94, no. 10, pp. 6697–6707, Nov. 2003.
[74] T. A. Pomorski *et al.*, "Defect structure and electronic properties of SiOC:H films used for back end of line dielectrics," *J. Appl. Phys.*, vol. 115, no. 23, Jun. 2014, Art. no. 234508.
[75] S. W. King, B. French, and E. Mays, "Detection of defect states in low-k dielectrics using reflection electron energy loss spectroscopy," *J. Appl. Phys.*, vol. 113, no. 4, Jan. 2013, Art. no. 044109.
[76] M. V. Fischetti, D. J. DiMaria, S. D. Brorson, T. N. Theis, and J. R. Kirtley, "Theory of high-field electron transport in silicon dioxide," *Phys. Rev. B*, vol. 31, no. 12, pp. 8124–8142, Jun. 1985.
[77] K. B. Yeap *et al.*, "Impact of electrode surface modulation on time-dependent dielectric breakdown," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2015, pp. 2A.1.1-2A.1.5.
[78] S. W. King, M. French, M. Jaehnig, M. Kuhn, and B. French, "X-ray photoelectron spectroscopy investigation of the Schottky barrier at low-k a-SiO(C):H/Cu interfaces," *Appl. Phys. Lett.*, vol. 99, no. 20, Nov. 2011, Art. no. 202903.
[79] J. M. Atkin, D. Song, T. M. Shaw, E. Cartier, R. B. Laibowitz, and T. F. Heinz, "Photocurrent spectroscopy of low-k dielectric materials: Barrier heights and trap densities," *J. Appl. Phys.*, vol. 103, no. 9, May 2008, Art. no. 094104.
[80] X. Guo *et al.*, "Measurements of Schottky barrier at the low-k SiOC:H/Cu interface using vacuum ultraviolet photoemission spectroscopy," *Appl. Phys. Lett.*, vol. 107, no. 23, Dec. 2015, Art. no. 232905.
[81] X. Guo *et al.*, "Defect-induced bandgap narrowing in low-k dielectrics," *Appl. Phys. Lett.*, vol. 107, no. 8, Aug. 2015, Art. no. 082903.
[82] D. J. DiMaria and J. W. Stasiak, "Trap creation in silicon dioxide produced by hot electrons," *J. Appl. Phys.*, vol. 65, no. 6, pp. 2342–2356, Mar. 1989.
[83] D. A. Buchanan, A. D. Marwick, D. J. DiMaria, and L. Dori, "Hot-electron-induced hydrogen redistribution and defect generation in metal-oxide-semiconductor capacitors," *J. Appl. Phys.*, vol. 76, no. 6, pp. 3595–3608, Sep. 1994.

[84] E. G. Liniger, S. A. Cohen, and G. Bonilla, "Low-field TDDB reliability data to enable accurate lifetime predictions," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2014, pp. BD.4.1-BD.4.4.
[85] K. Croes *et al.*, "Current understanding of BEOL TDDB lifetime models," *ECS J. Solid State Sci. Technol.*, vol. 4, no. 1, pp. N3094–N3097, Jan. 2015.
[86] F. L. Riley, "Silicon nitride and related materials," *J. Am. Ceram. Soc.*, vol. 83, no. 2, pp. 245–265, Feb. 2000.
[87] H. Klemm, "Silicon nitride for high-temperature applications," *J. Am. Ceram. Soc.*, vol. 93, no. 6, pp. 1501–1522, Jun. 2010.
[88] S. Veprek and M. J. G. Veprek-Heijman, "Industrial applications of superhard nanocomposite coatings," *Surf. Coat. Technol.*, vol. 202, no. 21, pp. 5063–5073, Jul. 2008.
[89] Z. Cheng, X. Huang, H. Huang, K. Wang, and G. Li, "Effect of arsenic doping on charge relaxation process in silicon nitride film for capacitive RF MEMS switch application," *Microelectron. Eng.*, vol. 162, pp. 89–92, Aug. 2016.
[90] A. Masuda, H. Umemoto, and H. Matsumura, "Various applications of silicon nitride by catalytic chemical vapor deposition for coating, passivation and insulating films," *Thin Solid Films*, vol. 501, no. 1, pp. 149–153, Apr. 2006.
[91] E. Suzuki, H. Hiraishi, K. Ishii, and Y. Hayashi, "A low-voltage alterable EEPROM with metal-oxide-nitride-oxide-semiconductor (MONOS) structures," *IEEE Trans. Electron Devices*, vol. 30, no. 2, pp. 122–128, Feb. 1983.
[92] S. Choi *et al.*, "Memory characteristics of silicon nitride with silicon nanocrystals as a charge trapping layer of nonvolatile memory devices," *Appl. Phys. Lett.*, vol. 86, no. 25, Jun. 2005, Art. no. 251901.
[93] K. Kobayashi, A. Suzuki, and K. Ishikawa, "Thermal annealing effect on ultraviolet-light-induced leakage current in low-pressure chemical vapor deposited silicon nitride films," *Thin Solid Films*, vol. 550, pp. 545–553, Jan. 2014.
[94] H. Matsumura *et al.*, "Highly moisture-resistive SiN_x films by catalytic chemical vapor deposition and their application to passivation and antireflection coating for crystalline Si solar cells," in *Proc. 3rd World Conf. Photovoltaic Energy Conversion*, vol. 2, 2003, pp. 1147–1150.
[95] S. W. King *et al.*, "Film property requirements for hermetic low-k a-$SiO_xC_yN_z$:H dielectric barriers," *ECS J. Solid State Sci. Technol.*, vol. 1, no. 6, pp. N115–N122, Jan. 2012.
[96] S. Fujita and A. Sasaki, "Dangling bonds in memory-quality silicon nitride films," *J. Electrochem. Soc.*, vol. 132, no. 2, pp. 398–402, Feb. 1985.
[97] J. Robertson, "Electronic structure of silicon nitride," *Philos. Mag. Part B*, vol. 63, no. 1, pp. 47–77, Jan. 1991.
[98] J. Robertson, "Defects and hydrogen in amorphous silicon nitride," *Philos. Mag. Part B*, vol. 69, no. 2, pp. 307–326, Feb. 1994.
[99] H. Cui and P. A. Burke, "Time-dependent dielectric breakdown of hydrogenated silicon carbon nitride thin films under the influence of copper ions," *Appl. Phys. Lett.*, vol. 84, no. 14, pp. 2629–2631, Apr. 2004.
[100] M. J. Mutch, P. M. Lenahan, and S. W. King, "Spin transport, magnetoresistance, and electrically detected magnetic resonance in amorphous hydrogenated silicon nitride," *Appl. Phys. Lett.*, vol. 109, no. 6, Aug. 2016, Art. no. 062403.

[101] Y. Shi, X. Wang, and T.-P. Ma, "Electrical properties of high-quality ultrathin nitride/oxide stack dielectrics," *IEEE Trans. Electron Devices*, vol. 46, no. 2, pp. 362–368, Feb. 1999.
[102] R. Degraeve *et al.*, "New insights in the relation between electron trap generation and the statistical properties of oxide breakdown," *IEEE Trans. Electron Devices*, vol. 45, no. 4, pp. 904–911, Apr. 1998.
[103] S. P. Ogden, J. Borja, J. L. Plawsky, T.-M. Lu, K. B. Yeap, and W. N. Gill, "Charge transport model to predict intrinsic reliability for dielectric materials," *J. Appl. Phys.*, vol. 118, no. 12, Sep. 2015, Art. no. 124102.
[104] S. W. King, M. French, M. Jaehnig, M. Kuhn, B. Boyanov, and B. French, "X-ray photoelectron spectroscopy measurement of the Schottky barrier at the SiC(N)/Cu interface," *J. Vac. Sci. Technol. B*, vol. 29, no. 5, Sep. 2011, Art. no. 051207.
[105] C. M. Osburn and D. W. Ormond, "Dielectric breakdown in silicon dioxide films on silicon – I . Measurement and interpretation," *J. Electrochem. Soc.*, vol. 119, no. 5, pp. 591–597, May 1972.
[106] I.-C. Chen, S. E. Holland, and C. Hu, "Electrical breakdown in thin gate and tunneling oxides," *IEEE J. Solid-State Circuits*, vol. 20, no. 1, pp. 333–342, Feb. 1985.
[107] H. Zhou, F. G. Shi, and B. Zhao, "Thickness dependent dielectric breakdown of PECVD low-k carbon doped silicon dioxide dielectric thin films: modeling and experiments," *Microelectron. J.*, vol. 34, no. 4, pp. 259–264, Apr. 2003.
[108] K. C. Kao, C. J. Huang, C. S. Wu, and Y. L. Cheng, "Thickness dependence on electrical and reliability properties for dense and porous low dielectric constant materials," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2015, pp. BD.6.1-BD.6.4.
[109] J. W. McPherson, "On why dielectric breakdown strength reduces with dielectric thickness," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2016, pp. 3A.3.1–3A.3.8.
[110] S. P. Ogden, Y. Xu, K. B. Yeap, T. Shen, T.-M. Lu, and J. L. Plawsky, "Charge transport model to predict dielectric breakdown as a function of voltage, temperature, and thickness," *J. Appl. Phys.*, submitted for publication.
[111] S. P. Ogden, T.-M. Lu, and J. L. Plawsky, "Electron transport and dielectric breakdown in silicon nitride using a charge transport model," *Appl. Phys. Lett.*, vol. 109, no. 15, Oct. 2016, Art. no. 152904.
[112] J. W. McPherson, "Determination of the nature of molecular bonding in silica from time-dependent dielectric breakdown data," *J. Appl. Phys.*, vol. 95, no. 12, pp. 8101–8109, Jun. 2004.
[113] H. Fröhlich and B. V. Paranjape, "Dielectric breakdown in solids," *Proc. Phys. Soc. Sect. B*, vol. 69, no. 1, pp. 21-32, 1956.
[114] M. V. Fischetti, S. E. Laux, and E. Crabbé, "Understanding hot-electron transport in silicon devices: Is there a shortcut?," *J. Appl. Phys.*, vol. 78, no. 2, pp. 1058–1087, Jul. 1995.
[115] P. E. Cottrell, R. R. Troutman, and T. H. Ning, "Hot-electron emission in n-channel IGFETs," *IEEE J. Solid-State Circuits*, vol. 14, no. 2, pp. 442–455, Apr. 1979.
[116] E. Takeda, H. Kume, T. Toyabe, and S. Asai, "Submicrometer MOSFET structure for minimizing hot-carrier generation," *IEEE Trans. Electron Devices*, vol. 29, no. 4, pp. 611–618, Apr. 1982.

[117] S. Tam, F. C. Hsu, C. Hu, R. S. Muller, and P. K. Ko, "Hot-electron currents in very short channel MOSFET's," *IEEE Electron Device Lett.*, vol. 4, no. 7, pp. 249–251, Jul. 1983.
[118] S. Tam, P.-K. Ko, and C. Hu, "Lucky-electron model of channel hot-electron injection in MOSFET'S," *IEEE Trans. Electron Devices*, vol. 31, no. 9, pp. 1116–1125, Sep. 1984.
[119] W. M. Deen, *Analysis of Transport Phenomena*, 2nd ed. New York, NY, USA: Oxford University Press, 2012.
[120] F. Chen, M. A. Shinosky, and J. M. Aitken, "Extreme-value statistics and poisson area scaling with a fatal-area ratio for low-k dielectric TDDB modeling," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3089–3098, Sep. 2011.
[121] S. P. Ogden, K. B. Yeap, T. Shen, P. Justison, T.-M. Lu, and J. L. Plawsky, "Method to determine the root cause of low-κ SiCOH dielectric failure distributions," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 119–122, Jan. 2017.
[122] G. S. Haase, E. T. Ogawa, and J. W. McPherson, "Reliability analysis method for low-k interconnect dielectrics breakdown in integrated circuits," *J. Appl. Phys.*, vol. 98, no. 3, Aug. 2005, Art. no. 034503.
[123] F. Chen, P. S. McLaughlin, and K. Chanda, "Nondestructive electrical characterization of integrated interconnect line-to-line spacing for advanced semiconductor chips," *Appl. Phys. Lett.*, vol. 91, no. 19, Nov. 2007, Art. no. 192109.
[124] F. Chen *et al.*, "Line edge roughness and spacing effect on low-k TDDB characteristics," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2008, pp. 132–137.
[125] S. C. Lee, A. S. Oates, and K. M. Chang, "Geometric variability of nanoscale interconnects and its impact on the time-dependent breakdown of Cu/low-k dielectrics," *IEEE Trans. Device Mater. Reliab.*, vol. 10, no. 3, pp. 307–316, Sep. 2010.
[126] W. L. Warren, J. Kanicki, J. Robertson, and P. M. Lenahan, "Energy level of the nitrogen dangling bond in amorphous silicon nitride," *Appl. Phys. Lett.*, vol. 59, no. 14, pp. 1699–1701, Sep. 1991.
[127] F. Chen and M. Shinosky, "Electron fluence driven, Cu catalyzed, interface breakdown mechanism for BEOL low-k time dependent dielectric breakdown," *Microelectron. Reliab.*, vol. 54, no. 3, pp. 529–540, Mar. 2014.
[128] R. S. Achanta and P. McLaughlin, "A charge transport based acceleration model for interlevel dielectric breakdown," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2011, pp. BD.2.1-BD.2.5.
[129] E. Y. Wu, B. Li, and J. H. Stathis, "Modeling of time-dependent non-uniform dielectric breakdown using a clustering statistical approach," *Appl. Phys. Lett.*, vol. 103, no. 15, Oct. 2013, Art. no. 152907.
[130] E. Y. Wu, B. Li, J. H. Stathis, and C. LaRow, "Time-dependent clustering model versus combination-based approach for BEOL/MOL and FEOL non-uniform dielectric breakdown: Similarities and disparities," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2014, pp. 5B.2.1-5B.2.7.
[131] K. Fischer *et al.*, "Low-k interconnect stack with multi-layer air gap and tri-metal-insulator-metal capacitors for 14nm high volume manufacturing," in *Proc. IEEE*

Int. Interconnect Tech. Conf. and Materials for Advanced Metallization Conf. (IITC/MAM), 2015, pp. 5–8.