60 Gs/s Analog-to-Digital Conversion in SiGe HBT Technology

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ABSTRACT

The goal of this research was to design, implement and test an ultra high speed SiGe analog to digital converter (ADC). High speed ADC's have uses in many areas, including digital oscilloscopes, front ends for software defined radio, as well as digital radar. With sufficient sampling rates, ADC's can be pushed to the front end of a receiver, eliminating the need for analog circuits and providing the flexibility to receive a much wider range of frequencies while consuming less power and layout size.

An open loop, scalable, time-interleaved ADC architecture is presented in this thesis. With the use of double-sampling, the timing skew requirements between channels is greatly relaxed, allowing sampling rates of up to 60Gs/s at 4-bits of accuracy.

This thesis will focus on the major components of the ADC system, as well as oscillator design. The impact of clock jitter on ADC performance is analyzed, with discussion on the purity of clock source needed for achieving more accuracy at ultra high speeds. Several test chips have been fabricated to test the performance of critical sub-components used in the ADC design.

Future work includes investigation of increased interleaving to reduce single channel speeds so that resolution can be increased, as well as substituting CMOS logic in the backend of the converter to lower power consumption and layout size. This circuit is currently faster than any published designs, and is implemented using the IBM 8HP SiGe technology, with fT of 210GHz.