PERFORMANCE OF THROUGH STRATA VIAS (TSVS) IN THREE-DIMENSIONAL INTEGRATION

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ABSTRACT

Emerging three-dimensional (3D) integration has become a key enabling technology as we face both serious challenge with device/interconnect scaling and increasing demand for on-chip functionality. 3D technology can offer benefits of the speed, signal integrity, power consumption, size, and yield. Owing to its short wiring and high density, through-strata-via (TSV) is regarded as an essential component in three-dimensional integration and packaging in order to extend Moore's Law scaling with CMOS technology. Consequently, it is important to investigate and predict the electrical performance of TSVs. This work discusses integration of TSV technologies, and presents evaluation and modeling of electrical performance using a commercially available simulator.

A variety of TSV fabrication processes in 3D integration are surveyed and compared, along with some thermo-mechanical simulation results. Three common types of techniques implemented in electromagnetic full wave simulators are discussed. TSV electrical characteristics are explored based on physical configurations and materials. Return loss S_{11}, and forward gain S_{21} are simulated up to 20 GHz using Agilent's ADS. Current density contour and radiation pattern of TSV structure are shown. Moreover, analytical techniques in the time domain like Time Domain Reflectometry/Transmissometry (TDR/TDT) and the eye diagram are employed to estimate noise and loss. From TDR/TDT simulation, the rise time becomes slow when a step pulse travels through the TSV structure. As data rate increases, the eye opening shrinks, i.e., voltage and time margins are reduced. For a specific TSV configuration, the effect of changing parameters are examined. Trace length dominates the reflection noise and signal gain of the whole structure, while the impact of trace width and thickness are small. Neither big nor small TSV is a good choice owing to the tradeoff between geometrically-determined liner capacitance and via resistance. Copper and tungsten filling show close results, whereas the polysilicon TSV shows a degradation of S_{11} and S_{21}. A partially filled via shows better performance than a solid one. High resistivity silicon can reduce the coupling paths at high frequency,

while thin substrates reduce TSV parasitics. While measured resistance, inductance and capacitance data are collected from literature, a harmonic balance simulation is used to extract the TSV parasitics for a specially constructed TSV structure. For a 4-port network built, equivalent TSV circuit models are proposed, and then values of passive elements of R, L and C are extracted from scattering parameters obtained in the schematic simulator. The extracted values of passive elements agree well with the theortical calculation. From these initial results and preliminary design guidelines, S_{11} and S_{21} in the network could be improved, leading to enhanced performance of 3D circuits and systems.