High-Performance Memory Systems using 3D IC Technology

by

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ABSTRACT

Although the continuation of Moore's law has resulted in sustained growth in microprocessor speed for many years, improvements in speed and performance of CMOS memory systems have been far from satisfactory. In fact, the performance gap between the CPU and memory subsystem has been continuously widening. In this work, we investigate using the 3D integration technology in bridging this gap. Firstly, a performance comparison between 2D and 3D SRAM is performed where it is concluded that although 3D integration does improve wire delay in memory structures, the improvement does not have a very significant effect on its access time. It is argued that the major benefit of 3D stacking is in terms of realizing a very wide data bus between CPU and memory system. Towards that end, a three-tier, 3D 192-KB unified L2 cache chip is designed and fabricated in a 0.18-um fully-depleted SOI CMOS process. An ultra wide data bus for connecting the 3D L2 cache with the lower level L1 cache is implemented using dense vertical vias between the stacked wafers. The cache operates at 500 MHz and achieves up to 96 GB/s aggregate bandwidth. In the final part of the thesis, design of a very high-density 3D SOI 1T DRAM with floating body cell (FBC) is investigated. Such a capacitor-less DRAM, which when stacked on top of the CPU and cache, might eliminate the need of external main memory. Operating conditions of the capacitor-less 1T FBC DRAM are analyzed and robustness studies are carried out. A test chip has been designed and fabricated to characterize and validate its operation.