CIRCUIT AND SYSTEM DESIGN FOR MAGNETORESISTIVE DIGITAL MEMORY AND CACHE

By

Wei Xu

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Examining Committee:

Tong Zhang, Thesis Adviser
Gary J. Saulnier, Member
Partha Dutta, Member
Saroj Nayak, Member

Rensselaer Polytechnic Institute
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ABSTRACT

Spin-torque transfer (STT) magnetoresistive memory has been widely considered as one of the most promising universal memory technologies, because of its many desirable attributes including non-volatility, high storage density, superior scalability, low integration cost and high access speed. However, most recent and on-going research mainly focus on the fabrication, device modeling, and/or memory circuit design, while research from architecture and system perspectives remain largely missing. In this thesis, we intend to jointly consider memory device, circuit, architecture, and systems in order to most synergetically exploit the potential of STT memory in real-life applications.

First, we focus on cell structure design for STT magnetoresistive random access memory (RAM), content addressable memory (CAM) and ternary CAM (TCAM). Most prior work on magnetoresistive RAM (MRAM) circuit design employs a compact 1MTJ/cell structure and a current mode sensing scheme, which tends to result in relatively complex and large peripheral circuits. Moreover, due to the more severe constraint in STT MRAM, it can be more challenging to apply this sensing scheme to realize high-speed read in STT MRAM. A 2MTJ/cell structure, which applies a voltage mode sensing scheme, has been used to improve the read speed, but results in much larger cell area than a simple 1MTJ/cell structure. We propose a new STT MRAM structure that applies the same voltage mode sensing scheme to improve the sensing speed and reliability, while using only one MTJ and one transistor in each cell. Using the same design principle, we further develop MTJ-based cell structures for non-volatile CAM and TCAM. The effectiveness of the proposed RAM, CAM and TCAM cell structures has been demonstrated by circuit simulation at 0.18μm CMOS technology.

Secondly, we propose a technique to improve the storage density of STT MRAM in the presence of significant MTJ write current threshold variability. In conventional design practice, the nMOS transistor within each memory cell is sized to be large enough to carry a current larger than the worst-case MTJ write current

threshold, leading to an increasing storage density penalty as the technology scales down. To mitigate such variability induced storage density penalty, we present a smaller-than-worst-case transistor sizing approach with the underlying theme of jointly considering memory cell transistor sizing and defect tolerance. Its effectiveness is demonstrated using 256Mb STT MRAM design at 45nm node as a test vehicle. Results show that, under a normalized write current threshold deviation of 20%, the overall memory die size can be reduced by more than 20% compared with the conventional worst-case transistor sizing design practice.

Finally, we explore the potential of STT MRAM to replace SRAM as last-level on-chip cache (e.g., L2 or L3 cache) for microprocessors. Due to unique operational characteristics of its storage device MTJ, STT MRAM is inherently subject to a write latency vs. read latency trade-off that is determined by the memory cell size. We first quantitatively study how different memory cell sizing may impact the overall computing system performance, and show that different computing workloads may have conflicting expectations on memory cell sizing. Leveraging MTJ device switching characteristics, we further propose an STT MRAM architecture design method that can make STT MRAM cache with relatively small memory cell size perform well over a wide spectrum of computing benchmarks. This has been well demonstrated using CACTI-based memory modeling and computing system performance simulations using *SimpleScalar*. Moreover, we show that this design method can also reduce STT MRAM cache energy consumption by up to 30% over a variety of benchmarks.