3D LOGIC-MEMORY INTEGRATION FOR HIGH PERFORMANCE EMBEDDED SYSTEM AND RECONFIGURABLE COMPUTING

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Three-dimensional (3D) integration has recently become a topic of great interest because of its many compelling advantages such as increased performance, reduced power, small form factor, flexible heterogeneous integration, and reduced overall costs. We proposed two approaches to improvement the system performance by 3D Memory-Logic integration. The first approach studies the potential of using emerging 3D integration to improve embedded VLIW computing system. We focus on the 3D integration of one VLIW processor die with multiple high-capacity DRAM dies. Our proposed memory architecture employs 3D stacking technology to bond one die containing several processing clusters to multiple DRAM dies for a primary memory. The 3D technology also enables wide low-latency buses between clusters and memory and enable the latency of 3D DRAM L2 cache comparable to 2D SRAM L2 cache. These enable it to replace the 2D SRAM L2 cache with 3D DRAM L2 cache. The die area for 2D SRAM L2 cache can be re-allocated to additional clusters that can improve the performance of the system. From the simulation results, we find 3D stacking DRAM main memory can improve the system performance by 10%∼80% than 2D off-chip DRAM main memory depending on different benchmarks. Also, for a similar logic die area, a four clusters system with 3D DRAM L2 cache and 3D DRAM main memory outperforms a two clusters system with 2D SRAM L2 cache and 3D DRAM main memory by about 10%.

The second approach is the emerging three-dimensional (3D) integration technologies can naturally meet this demand by enabling 3D FPGA-memory integration. As FPGAs enter increasingly diverse and high-end applications, large on-chip storage capacity with high memory bandwidth becomes increasingly indispensable. The 3D stacked memory may hold both embedded memory blocks visible to the users and multiple sets of FPGA configurations. We propose and study a DRAM-based FPGA design strategy enabled by such 3D FPGA-memory integration. In current design practice, FPGAs do not use on-chip DRAM cells for configuration data storage mainly because on-chip DRAM self-refresh involves destructive DRAM read operations. This problem can be solved if we use the 3D stacked memory as primary FPGA configuration data storage and externally refresh on-chip DRAM cells. In this work, we study such DRAM-based FPGA design and investigate involved

design issues, and employ the VPR tool set to demonstrate that DRAM-based FPGAs can noticeably reduce FPGA die area and hence improve speed and dynamic power consumption performance, compared to their SRAM-based counterparts.