ELECTRICAL EVALUATION AND MODELING OF THROUGH-STRATA-VIAS (TSVS) IN THREE-DIMENSIONAL (3D) INTEGRATION

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ABSTRACT

Three-dimensional (3D) integration, which stacks and connects function blocks vertically, can overcome some physical/technological/economic limits encountered in planar ICs. A key component in 3D integration technology is the through-strata-via (TSV); a massive number of short TSVs can electrically connect multiple strata of ICs vertically, enabling high performance, high functionality, compact heterogeneous systems with high data bandwidth and speed, and low power and cost. Although substantial research is being conducted on other aspects of TSVs, critical research is needed to examine the TSV electrical properties for a wide range of TSV types so that their suitability for specific applications can be evaluated and 3D design facilitated. The objective of this thesis is to investigate TSV electrical performance.

Based on study of a wide variety of TSV fabrication processes, configurations, implementations and applications, TSV electrical performance is systematically examined with numerical/analytical simulation and modeling methods. Electrical characteristics of a baseline signal-ground Cu TSV pair (10 μm in diameter, 20 μm in pitch, 30 μm in height, 0.1 μm thick SiO_2 isolation layer, 10 Ω-cm in thinned Si substrate resistivity) are simulated in the frequency domain and time domain using field solvers. TDR/TDT results show little degradation in the rise time, and the Z_{load} curve suggests TSV capacitive characteristics. A wide and high eye pattern indicates adequate time and voltage margins, and a very low level (10^{-17}) of bit error rate (BER) is observed in the 3D bathtub plot. TSV down-scaling can greatly improve performance. Among different TSV shapes, the tapered-shape TSV is preferred in terms of both electrical performance and fabrication. The partially-filled TSV can electrically perform the same as the solid one.

Various parametric tunings are conducted for three TSV physical configurations: (1) metal pads and solder balls associated with TSVs, (2) coaxial TSV materials and geometries, and (3) crosstalk estimation in high-density TSV networks. Instead of using multiple small TSVs sharing a common pad, it is better to implement one single big TSV where undesired couplings disappear and signal

gain increases by 20%. Impact of solder sizes (e.g., 25 - 100 μm) is negligible, and multiple layer stacking significantly degrades S_{21} and eye diagrams. A novel coaxial TSV has superior electrical performance (over 60% enhancement) to other TSVs. All the metals (except for Ni) show very similar results, and a thick low-k tubular dielectric with a small loss tangent is preferred. Slowing the rise time, enlarging the TSV pitch and shortening the TSV height help reduce the crosstalk noise. A high resistivity substrate is more favorable for crosstalk control. The voltage patterns on the aggressor TSVs vary the time delay and crosstalk level of the victim TSV.

Ten extraction techniques are explored to investigate TSV parasitics, including a 3D fullwave electromagnetic (EM) simulator, 3D quasi-static EM simulator, SPICE simulator, and analytical methods. The resulting values of RLGC per unit length are in the order of mΩ/μm, pH/μm, μS/μm and fF/μm, respectively. Several SPICE wideband modeling approaches are applied to match the fullwave EM scattering matrix with the fitting errors less than 0.05%. A sensitivity analysis indicates that the isolation layer thickness affects the TSV performance most and the down-scaling of TSV dimensions improves the performance. Furthermore, with a partition and assembly method, a hybrid simulation approach combining EM and SPICE simulators is proposed to examine a TSV-based 3D power network. Quantitative intuitions for 3D power network built-up and floorplanning are obtained under the worst-case scenarios.

The approaches developed in this work to evaluating and modeling the TSV electrical performance and the quantitative benefits and tradeoffs obtained for various TSV configurations provide the tool boxes and guidelines for developing 3D integration technologies and products.