# SYSTEM ARCHITECTURE DESIGN FOR HIGH PERFORMANCE THREE-DIMENSIONAL MEMORY SYSTEM AND SOLID STATE DRIVE STORAGE SYSTEM

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# ABSTRACT

In order to solve the memory wall problem at the main memory level and the storage level, we propose several design approaches based on three-dimensional (3D) memory-logic integration and solid state drive (SSD) techniques to increase the performance of the computing system.

At the main memory level, we first study the potential of using emerging 3D integration to improve embedded VLIW computing system. Our proposed memory architecture employs 3D stacking technology to bond one die containing several processing clusters to multiple DRAM dies for a primary memory. The design also replaces the 2D SRAM L2 cache with 3D DRAM L2 cache. The die area for 2D SRAM L2 cache can be re-allocated to additional clusters that can improve the performance of the system. The second approach is to replace the SRAM cells of FPGA with DRAM cells, enabled by the 3D integration technologies, to reduce the area and increase the performance.

At the storage level, it is well known that NAND flash memory program/erase (PE) cycling gradually degrades memory device raw storage reliability. Memory manufacturers must fabricate enough number of redundant memory cells geared to the worst-case device reliability at the end of memory lifetime. Given the memory device wear-out dynamics, the existing worst-case oriented ECC redundancy is largely under-utilized over the entire memory lifetime. We advocate a device-aware adaptive system design strategy to improve various NAND flash memory system performance metrics and memory defect tolerance. In addition, we present a quasi-nonvolatile SSD design strategy to trade data retention time of NAND flash memory for other system performance metrics including endurance and system performance, and meanwhile use explicit internal data refresh to accommodate very short data retention time with negligible energy consumption. At last, all the existing algorithms aim to equalize the erase number among all the memory blocks. Unfortunately, such a conventional design practice becomes sub-optimal as inter-block variation becomes increasingly significant with the technology scaling. We present a dynamic bit error rate(BER) based greedy wear-leveling algorithm to fully maximize the wear-leveling efficiency.