CIRCUIT AND SYSTEM DESIGN FOR SHINGLED MAGNETIC RECORDING

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ABSTRACT

Engineering research towards increasing the areal density in magnetic data storage are now facing numerous technological challenges. Overcoming these limitations has been the highlight of technological innovation of the storage industry. Magnetic recording systems have always been one of the most challenging domains where inter-disciplinary expertise is mandatory. The most promising technology, which can make it easier to surmount the areal density barrier is shingled magnetic recording (SMR). The thesis highlights the importance of using a multitude of characteristics of magnetic data storage, to help alleviate the problems faced by moving towards higher areal densities using SMR.

Specifically, SMR uses an overlap writer to reduce the track pitch; thereby providing a gain in the areal density. This comes with penalties of a preclusion of an update-in place operation and the presence of increased inter-track interference (ITI). The thesis presents intuitive and simple techniques to work with these issues and still achieve the required areal densities. To handle the preclusion of an update-in place operation along with severe ITI, three major techniques have been developed. First, we propose to apply dynamic spin speed boost to reduce the net latency incurred, which takes into account the penalties involved in the channel and system model. Then the study considers a 2D, 1-sided read channel processing strategy in order to save an additional rotational latency. The introduction of a head offset with the main track center, which is atypical for a conventional disk drive, is shown to provide signal-to-noise ratio (SNR) and performance benefits. Finally, the thesis proposes a most recently used (MRU) shingle strategy that minimizes the latency by over an order of magnitude for most workloads.

Compression has been widely discussed in open literature to reduce storage capacity and storage bandwidth. The thesis investigates the potential of using data compression to effectively minimize the random read latency in the presence of ITI. The principle is that, for SMR to work with a single read head, a progressive just-enough signal processing is required. The study presents a transparent intra-sector

compression scheme, which provides significant savings. Subsequently, the thesis develops a virtual sector design strategy to further improve the effectiveness. The virtual sector takes into account the read and update operations due to the banded structure, and it will incur marginal performance loss by compressing multiple sectors together but provide significant gains in SNR. Finally, the thesis presents a content aware approach, which uses the knowledge of the type of data to fix a suitable virtual sector size.

SMR creates a new operation space, which consists of the read/write and update operation that has to be handled. The scheduling of update operation is crucial for SMR drive operation. Since the read/write and update operation have asymmetric latencies, a simple partial update strategy is proposed to eliminate any excessive read latency that could be incurred. This is then furthered by looking into strategies for spatio-temporal coalescing, which aims to group request in the spatial and temporal domain corresponding to specific bands of data improving latency performance. Lastly an intuitive shortest update first algorithm is shown to provide performance gains to alleviate the update-latency issues . This algorithm also ensures the maximum number of update operations that are completed in a given span of time for a causal system architecture.

Finally, due to the severe ITI, SMR drives inevitably have considerable amount of retry-read operations in contrast to conventional disk drives. The thesis presents techniques that leverage multiple localized I/O's to reduce the average latency incurred due to retry-read. The thesis develops an inclusive-retry algorithm to reduce the impact of these retry effects, which provides significant benefits in the reduction of the overhead caused due to ITI. The thesis further developed a technique to achieve read latency reduction through channel processing emulation.