High Speed On-chip Interconnect Modeling and Reliability Assessment

by

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ABSTRACT

This thesis presents a CAD-oriented modeling for on-chip microstrip and coplanar-strip interconnect. Two improved model have been developed and several test structures have been designed and fabricated in a SiGe BiCMOS technology. The modeling technique uses a SPICE-friendly equivalent circuit approach which takes into account the wire skin effect and silicon substrate effect. The fully scalable ladder network contains only frequency-independent passive devices whose values are determined by geometry and technology specifications. It can be easily incorporated into standard industry simulation tools and migrated among various design environments. The numerical simulation results have been provided as well as the measured S-parameters, which are used to verify the model by extracting the RLGC parameters in the classical transmission line approach up to 50GHz.

This thesis also presents a methodology to do signal net electromigration and Joule heating analysis. A tool to filter signal nets to identify potential electromigration and Joule heating violation has been developed. A new approach to do static detailed analysis using linear solver has been explored. Future plans to enhance and complete the modeling and reliability checking work have been proposed.