High Speed Serial Data Transmission Integrated Circuits with Half-Rate Clock and Quarter-Rate Clock in SiGe BiCMOS Technology

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ABSTRACT

High-speed serial communication technology is in great demand to keep pace with the explosive increase of the data rate in digital data communication. The goal of this work is to design a leading edge high-speed serial data transmission circuitry utilizing a 0.13-μm SiGe BiCMOS technology. Two different clocking approaches are made to investigate possibilities. A 52-Gb/s 16:1 quarter-rate transmitter and a 66-Gb/s 4:1 half-rate transmitter are designed, fabricated, tested, and then compared. Both the transmitters achieve higher data rates than the state of the art with less power consumption.

The 16:1 quarter-rate transmitter consists of a 16:1 multiplexer (MUX), a voltage-controlled ring oscillator, a phase-locked loop (PLL), a pseudo-random data generator, and an output amplifier. The voltage-controlled ring oscillator shows a wide tuning range from 12 to 23 GHz with hybrid control schemes and a low phase noise of –104.8 dBc/Hz at 1 MHz offset. The VCO phase noise is stabilized as –124.6 dBc/Hz at 1 MHz offset by a third-order PLL. A continuous model of the third-order PLL is developed and used to optimize loop filter parameters and to estimate the PLL performance in a simulation. The 16:1 MUX features quarter-rate clock multiplexing with the multi-phase output VCO. In the design of a 16:4 MUX, total transition delay is reduced with fewer transistors used. Edge-Channeling 4:1 multiplexer is used to alleviate a duty cycle problem.

The 4:1 half-rate transmitter consists of a 4:1 MUX, an LC VCO, a PLL, and a built-in testing circuit. A 40-GHz cross-coupled LC VCO is designed with a single symmetric high-Q inductor. A novel high-speed F/F, HLO F/F, is designed and compared with conventional designs. A symmetric high-speed 4:1 MUX is designed with newly proposed 2:1 high-speed retiming MUXs (HRO-MUXs). The HRO-MUX achieves bandwidth improvement due to high-speed data retiming. The 4:1 half-rate transmitter shows an output data rate of 66 Gb/s with a data duty cycle of 53% due to the HRO-MUXs. A simple bit-error rate (BER) testing is performed with a built-in ring-counter. Power consumption of the 4:1 half-rate transmitter even with a built-in testing data generator is no more than 1.57 W, which is less than that of state of the art.