Silicon Lateral Trench Power MOSFETs for Power IC Applications

by

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An Abstract of a Thesis Submitted to the Graduate

Faculty of Rensselaer Polytechnic Institute

in Partial Fulfillment of the

Requirements for the degree of

DOCTOR OF PHILOSOPHY

Major Subject: Electrical Engineering

The original of the complete thesis is on file

In the Rensselaer Polytechnic Institute Library

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April, 2008
(For Graduation May, 2008)

ABSTRACT

Lateral power MOSFETs have been the preferred choice for output power device in power ICs mainly because of their ease of integration and high switching speed. However, conventional lateral structures have the limitation of increased specific on-resistance as a result of the long drift layer needed to support high voltage. Attempts to improve the specific on-resistance by adopting trench technology have usually resulted in poor switching performance as a result of increased overlap capacitance. As switching frequency is increased in order to keep up with the increasing load requirements, the switching loss in the power MOSFET starts to become significant in comparison to the conduction loss. A Figure of Merit (FoM) defined as the product of the on-resistance and gate charge ($R_{on}\times Q_g$) is used as a comparison metric for power MOSFETs in such applications, where the first and second terms respectively represent the conduction loss and switching loss.

Two implementations of a novel trench based lateral power MOSFET structure have been proposed in this research work, one with a planar drain contact and the other with a poly-plug based drain contact. The devices are based on a shallow trench (~1.0μm) technology in order to make them more compatible with an integrated process. The device structures were designed and optimized using the 2-D numerical simulator MEDICI, and the key performance metrics such as specific on-resistance and gate charge were estimated. The effect of various physical design parameters such as the source mesa, oxide spacer and drain pillar widths on device performance were studied and quantified. The optimal device structure was designed to sustain a breakdown voltage of 80V, making it suitable for computer and telecom power supply applications which operate in the 48V input range. The proposed power MOSFETs are also capable of high side operation enabling implementation of a wide variety of circuit topology.

The planar drain lateral trench power MOSFET was fabricated in a junction-isolation technology and its performance characterized. The optimal design of the fabricated MOSFET has a specific on-resistance of 1.63 mOhm-cm^2 and a gate charge of 185 nC/cm^2 at a gate bias of 10V, which agree very well with the numerical simulations. The FoM for the device was 300 mOhm-nC, which is over 2X improvement on the best reported lateral trench power MOSFET in its voltage class. In the off-state, the MOSFET had a breakdown voltage of 60V. On-state performance of the power MOSFET in the high side configuration was experimentally characterized.

The extensibility of the proposed lateral trench power MOSFET structure to support higher voltages in the range of 250V was also explored. Analytical models were developed to represent the electrical behavior of the power MOSFET and implemented in MAST HDL for use in commercial circuit simulators. Steps to implement a full-fledged power IC technology based around the proposed lateral trench power MOSFET have also been provided.