High-Voltage Lateral MOS-Gated FETs in Gallium Nitride

by

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ABSTRACT

Gallium Nitride (GaN) is of interest for high-voltage and high-temperature devices due to its remarkable material properties like wide bandgap (3.4 eV), large critical electric field (3 MV/cm) and high electron mobility in AlGaN/GaN heterostructure. Furthermore, GaN high-voltage devices especially lateral MOS-gated FETs can be integrated with control circuits, microwave devices and optoelectronic devices on one single GaN chip for a variety of applications. This research examines the capability of GaN MOS-gated FETs for logic and high-voltage switching applications by focusing on developing high quality GaN MOS interface, normally-off inversion-mode GaN MOSFET and high-voltage GaN MOS-gated FETs.

The insulator-GaN interface quality is crucial in creating high performance GaN MOS-gated devices. GaN MOS capacitors were fabricated to evaluate and optimize GaN MOS interface. In this thesis, we developed a new GaN MOS process resulting in extremely low interface state density (3.8×10^{10} $cm^{-2}eV^{-1}$ at 0.19 eV below the conduction band) and more importantly decreasing tread from conduction band to middle bandgap, showing potential inversion-mode GaN MOSFET.

Subsequently we demonstrated the first enhancement-mode inversion-mode GaN MOSFETs. Field-effect mobility up to 167 $cm^2/V\text{-}s$ (17% of bulk mobility) has been extracted on 100 μm long channel MOSFETs on both p and n- GaN/sapphire substrate. This record achievement still stands after nearly three years. Hall measurements on GaN MOS-gated Hall bar indicate that GaN MOS can provide about 2-4X mobility and 2X channel carrier density as compared to SiC MOS, only 2-3X lower than that of silicon MOS. By connecting a positive threshold voltage MOSFET and a negative threshold voltage MOSFET, we demonstrated the first GaN NMOS inverter with good voltage transfer characteristics, indicating potential use of GaN MOSFETs for digital applications. The fabricated MOSFETs show no mobility orientation dependence within c-plane, no current collapse and clear short-channel effect on 2 μm channel length devices.

High-voltage, lateral RESURF (REduced SURface Field) n-channel GaN MOS-gated FETs were designed and optimized using two-dimensional simulations. Three structures namely conventional implanted RESURF MOSFET, novel EPI RESURF

MOSFET and novel hybrid RESURF MOS-HEMT were investigated. Both one-zone and two-zone RESURF devices were examined and compared.

We developed new processes, process architectures and sequence and fabricated the designed three MOS-gated FETS. All the fabricated devices show good DC characteristics with nice linear and saturation region. We achieved breakdown voltage up to 2.5 kV or specific on-resistance as low as 30 mΩ-cm^2 (V_G=30 V) on implanted RESURF MOSFETs. The first GaN EPI RESURF MOSFET utilizing epitaxial n-GaN layer as RESURF layer was experimentally demonstrated to avoid any low RESURF dose activation process. One-zone EPI RESURF MOSFET without etched RESURF lalyer shows best tradeoff between specific on-resistance (34 mΩ-cm^2 at V_G-V_T=20 V) and breakdown voltage (730 V). This device performance is significantly better than any previously reported GaN MOSFETs. The specific on-resistance is 2 times lower than the 1D silicon limit and comparable to the best reported SiC lateral MOSFETs for the same blocking voltage. One-zone EPI RESURF MOSFET with etched RESURF layer shows low gate leakage current (<1 nA), but lower breakdown voltage (620 V) with specific on-resisatnce of 74 mΩ-cm^2 (V_G-V_T=20 V). The first novel hybrid MOS-HEMT by incorporating AlGaN/GaN heterostructure into the drift region was experimentally demonstrated to further reduce the specific on-resistance to 20 mΩ-cm^2 (V_G=30 V).