Modeling and Characterization of Amorphous Silicon Thin Film Transistors

by

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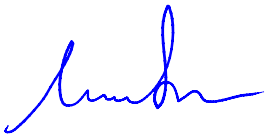
Approved: 

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ABSTRACT

The thesis presents modeling of capacitance-voltage characteristics of thin film transistors and thermal analysis of self-heating effects in thin film transistors and transistor arrays. The parameter extraction from C-V measurements is described and the limitations of the C-V characterization are discussed. The distributive nature of the capacitance in the device channel is shown to account for the capacitance frequency dispersion. To zero order, this effect can be reproduced by a lumped element equivalent circuit proposed by Elmore (the Elmore model) and by a new Variable Dispersion Model (VDM) accounting for finite interaction time between traps and states above the mobility edge. VDM has been developed and implemented in AIM-Spice. The combined VDM-Elmore model is shown to reproduce the entire dispersion observed in printed TFTs.

Dynamic thermal simulations for an amorphous Si TFT show that the temperature rise due to self heating can be noticeable (a few degrees for relatively short interconnects). We also present the dynamic thermal circuit for a TFT pixel that was simulated in Spice.

1. Introduction

1.1 Amorphous Silicon TFT technology

Amorphous Si TFTs have been employed in a wide range of macroelectronic applications wherein the focus is on large size and inexpensive fabrication. The applications of thin film transistors include large scale electronics such as flat panel displays in TVs, cellular phones, PDAs, camcorders, and laptop computers. The other applications include medical imagers, electronic and radio-frequency tags, image sensors [1], mechanical sensors [2], biological and chemical sensing [3] etc.

In 1972, Spear and LeComber fabricated amorphous silicon films with relatively low density of trap states in the energy gap. This material was an amorphous Si and hydrogen alloy, with a relatively high concentration of hydrogen. The hydrogen serves to tie up the dangling bonds in the amorphous silicon and hence leads to lower density of defect states in the bandgap. The first a-Si:H TFT was reported by LeComber et.al in 1979 [4]. Currently, amorphous Si continues to be the dominant technology in the flat panel display business.

Fig 1-1 shows that TFT based LCDs are the leading revenue source for the display industry and a-Si continues to be the most common TFT technology. The recent market research indicates that TFT based flat panel displays accounted for 85.4 % of the entire display market, contributing $21.8 Billion sales revenue in the second quarter of 2007 [5]. DisplaySearch forecasts TFT LCD revenue will increase to yearly revenue of $103.9 Billion in 2008. In 2007, the number TFT LCD TV shipped units equaled CRT TV shipped units for the first time and the near term future predictions state that large-sized TFT-LCD panel revenue is expected to reach $120.7 billion in 2012 [6]

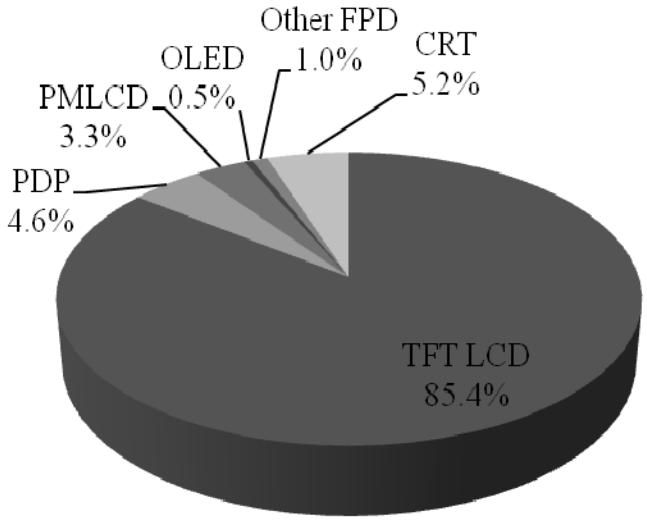

Figure 1-1: Display revenue share for Quarter 2 of 2007 from DisplaySearch [5]. Here "PDP" refers to "plasma display panel", PMLCD refers to "passive matrix LCD", other FPD refers to "other flat panel display technologies", and OLED refers to "Organic LED"

1.2 Review of advanced TFT technologies

In this section, a brief discussion of advanced TFT technologies is provided. Poly silicon TFT process was developed with the aim of integrating the drivers and the shift registers as well onto the same piece of glass. Low temperature laser annealing process is used to produce high performance poly Si TFTs. Mobility of around 100 cm^2/V.sec is common in poly Si TFTs. Recently, poly Si TFTs with novel device design having mobilities higher than 550 cm^2/V sec have been demonstrated [7]. A major advantage is that the higher electron and hole mobilities in poly-Si allow complementary devices to be fabricated for integrated display circuitry. However, the process for complementary poly Si TFTs is complex and needs a larger number of steps.

Despite the TFT size and performance advantages of low temperature poly-silicon, amorphous-silicon process continues to dominate the LCD panel market. This is due to the relatively lower cost of a-Si that results from fewer process steps and the unknowns associated with less mature LTPS equipment/process [8]. Consequently, poly-silicon TFTs are primarily used in smaller sized displays.

Organic thin film transistors provide a cost effective solution as compared to other technologies since they require low temperature processing steps for fabrication.

However, there are several problems associated with organic TFTs. The main problem is that organic TFTs suffer from mobility and threshold voltage shift with change in humidity levels [9].

Recently, TFTs have been fabricated on flexible substrates, instead of rigid glass substrates. These flexible TFTs open up new opportunities such as lightweight, unbreakable, and foldable display screens for computers and cell phones. Further, it can lead to electronic paper and paper like displays. Plastic substrates have emerged as a cheap option for flexible substrates. Further, the possibility of using printing techniques, instead of conventional lithography, has been a driving factor for adoption of flexible TFTs. The size of the glass substrate used in conventional TFTs has continued to increase, which leads to complicated photolithography and deposition steps. The solution lies in adopting high throughput printing process which do not require cost intensive lithography step.

Organic TFTs combined with cheap printing techniques can lead to the low cost, flexible displays and RFID tags. Hence, research focus has shifted to the development of printed organic TFTs in recent times. However, organic TFTs suffer from drift in characteristics due to exposure to moisture and other environmental factors. On the other hand, amorphous silicon TFTs are relatively stable to environmental factors and amorphous silicon processing is now a matured process. Recently, amorphous silicon transistors have been printed on flexible substrates using roll to roll printing techniques [15]. This process has high throughput and leads to cheaper productions of TFTs.

1.3 Active matrix LCD

Displays are made of pixels arranged in a matrix. When TFT is used to switch on individual pixel, the matrix is referred to as “active” matrix, while displays which do not use TFT switches are referred to as “passive” matrix. . As seen in fig 1-1, passive matrix LCD displays occupy a very small market share. They are simple to implement, but suffer from slow response time and imprecise voltage control and are not suited for large sized displays.

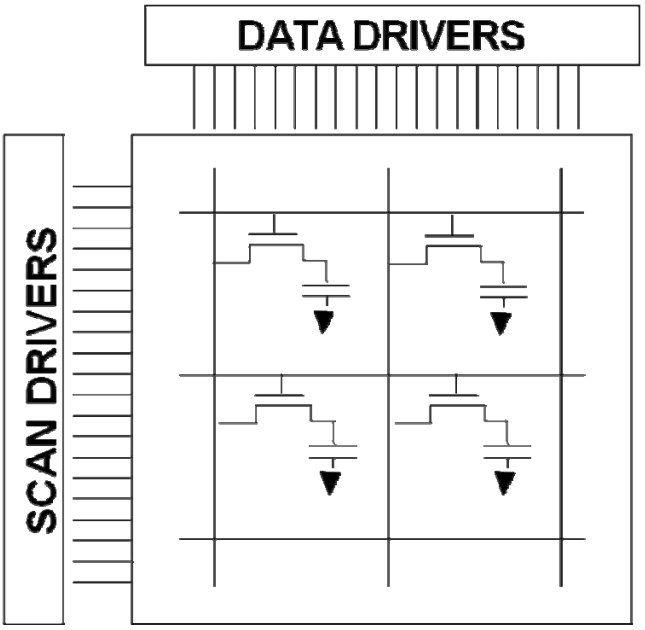

Figure 1-2: Schematic diagram showing the TFTs in an Active matrix Liquid crystal display [10]

In an Active Matrix LCD (AMLCD), TFT acts as a switch for controlling each pixel individually. Fig. 1-2 shows the schematic diagram of TFTs used as switches in AMLCD panel. The a-Si TFTs have faster response, low leakage current and a high on/off current ratio. However, the limitations with a-Si TFTs are low electron mobility (~1 cm^2/V sec) and the resolution limit of a-Si TFT LCDs due to the minimum size of the transistors.

In Liquid crystal display, the liquid crystal controls the amount of light passed though it, according to an applied voltage. TFT acts as a switch and controls the voltage level applied to each liquid crystal cell (pixel). A large number of these pixels are arranged in the form of a matrix to form complex images on the screen. In active matrix LCD, in order to select a row of pixels, on voltage is applied to the gates of all the TFTs in that particular row. A desired voltage is applied to these selected pixels using their respective column lines. The liquid crystal has capacitance associated with it, C_{LC}, and hence, the applied voltage leads to storage of charge in it. With the passage of time, this stored charge started leaking though the TFT and hence, the liquid crystal now allows more and more light to pass. Finally, when most charge is leaked, all light is allowed to pass. Hence, the charge in the liquid crystal has to be refreshed frequently. A storage capacitor C_s is also used in the pixel circuit, in order to store charge for a longer time,

leading to reduced refresh rates. Figure 1-3 shows the schematic of a pixel drive circuit for a TFT. When the gate input goes high, every TFT in the row is switched on. The drain current through each TFT is determined by the column voltage. These currents determine the charge on the capacitors – the liquid crystal capacitance (C_{LC}) and the storage capacitor (C_s).

This circuit is repeated in a large grid throughout the display. Each pixel row is activated in turn, and the columns charge the row's pixels to the appropriate grayscale for a given image. The flickering image appears continuous to the user because it is refreshed at a high rate. A 40~60 Hz refresh rate is typical.

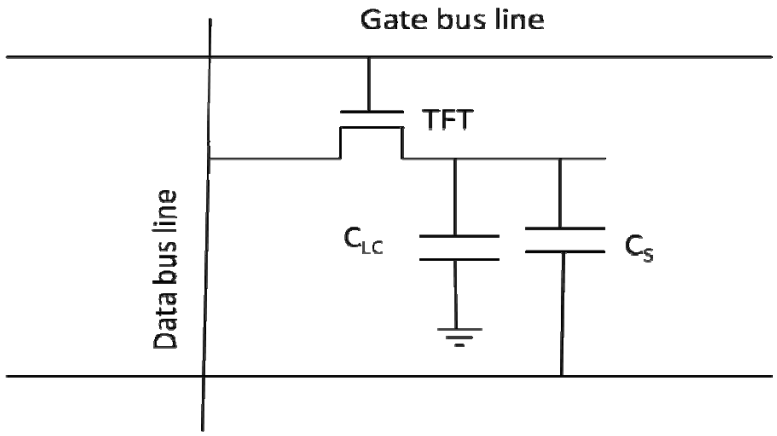

Figure 1-3: Schematic diagram showing one pixel circuit for a-Si TFT based active matrix addressing. C_{LC} represents the capacitance of the liquid crystal. C_s is the storage capacitor

1.4 TFT modeling and characterization

With wide-spread commercial success of conventional s-Si TFT and development of advanced printed amorphous Si TFTs, it has become of paramount importance to develop accurate, physics –based, compact models for these TFTs. The development of such models and modeling techniques will enable the industry to accurately estimate the performance and devise ways for improvement. Displays have become more complex and come in various sizes. The design of such wide range of displays needs robust models that can help predict the performance accurately. In addition to the displays, emerging application such RFIDs have pushed the development of new structures such as printed a-Si TFTs. Such developments have prompted development of newer models as well as improvements to the existing models.

Device models have become an important part of the manufacturing cycle. Accurate understanding of the various physical phenomena is important so that the simulations results are closer to the performance of the actual fabricated device. Accurate compact models can enable the designer to experiment with various designs in order to increase performance. It can also lead to faster design cycles and reduction of time to market. Further, enhanced understanding arising from these device models can help to identify steps towards increased reliability of the devices.

Device characterization can help to identify the problems occurring in the fabricated devices. In order to extract the various physical model parameters, characterization of the devices is essential. Further, characterization of a large number of devices can give an idea of the amount of variation occurring among TFTs fabricated on the same substrate as well as for shorter and longer gate length TFTs. Such information can then be included in the device model in order to more accurate simulation results.

For printed a-Si TFTs, the effect of non-ideal contacts and the disordered nature of the amorphous Silicon have to be considered for accurate device models. The dynamic self-heating during operation of the display, have to be considered in order to evaluate the effect in device reliability.

In this thesis, characterization methods for a-Si TFTs and modeling procedure for conventional a-Si TFTs on glass substrate is presented. A compact capacitance model for printed a-Si TFTs is developed and it has been shown to have a good agreement with the measured data. The dynamic thermal simulations of TFTs in a display matrix are presented.

There is a large body of work on modeling a-Si and poly-Si TFTs [11, 12, 29, 30]. However, the issues related to the frequency dispersion [13, 23] and thermal modeling received relatively little attention [39 ,51].

1.5 Organization of the thesis

The main goal of this thesis is to develop physics-based models that account for the physical effects in conventional and printed Amorphous Si TFTs. modeling and characterization of a-Si Thin Film transistors.

The introduction to a-Si TFT and discussion of the various applications such as Active Matrix LCDs, Active Matrix OLED displays and Radio frequency tags has been provided in Chapter 1.

In chapter 2, the characterization methods for a-Si TTs are presented. The I-V and C-V measurements are discussed, along with the errors and limitations of C-V measurements.

The basic TFT model for conventional TFTs is described in Chapter 3. This model is used for device modeling and modeling of ring oscillator circuit using conventional a-Si TFTs.

The new compact capacitance model for printed a-Si TFTs has been presented in Chapter 4. This is a new model implemented in AIM Spice as Level 33. The mathematical description of the frequency dispersion of capacitance is provided. The mechanism behind the gate length independent frequency dispersion, arising from the electron energy distribution time constant, has been discussed. The simulation of ring oscillator using this new model is presented.

The dynamic thermal simulations for a-Si based Active Matrix LCD displays are provided in Chapter 5. The thermal circuit for self-heating of TFTs under pulsed mode operation is provided and the effect of the position of the TFT within the display matrix on the temperature of the TFT is described.

2. Characterization of TFTs

In this chapter, we describe the structure of TFTs and the fabrication process used for the conventional a-Si TFTs as well as the printed a-Si TFTs used in this study. We present the measured I-V and C-V characteristics for both conventional and printed TFTs. We discuss the limitations and the errors involved in the characterization techniques.

2.1 TFT structures

The "inverted staggered" structure shown in Fig 2-1 is the most popular structure for a-Si TFTs. The inverted staggered structure is preferred because the nitride-amorphous Si interface has lower density of trap states when the nitride is deposited first and then the amorphous Si layer is deposited on top of the nitride [14]. The two types of inverted staggered a-Si:H TFTs, which differ slightly in their fabrication steps, are shown schematically in Figure 2-1 (a) and (b). The two structures (a) and (b) differ mainly in the order of deposition of n+ contacts and top-passivation nitride. Structure (a) has relatively simpler fabrication process, but structure (b) has lower photo sensitivity. For the fabrication of the TFT (a) structure, there is deposition of gate insulator, intrinsic a-Si:H and n+ a-Si:H in consecutive growth steps. The n+ a-Si:H is then etched from the channel region of the transistor. During the fabrication of the TFT (b), there is a consecutive deposition of gate insulator and intrinsic a-Si:H. In the following step, a second insulating layer (usually silicon nitride) which acts as a passivating layer is deposited over the a-Si channel. Later, the top insulator is etched from the contact regions and the doped layer for source and drain contacts is deposited.

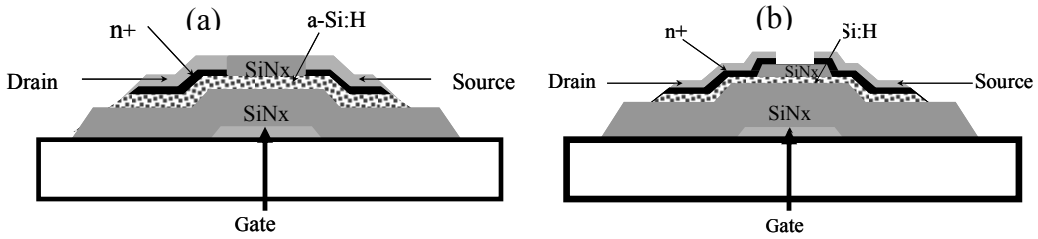

Figure 2-1: Inverted staggered structures for amorphous Silicon Thin Film Transistors: (a) Inverted staggered, unpassivated structure; (b) Inverted staggered, passivated structure

The inverted staggered a-Si TFTs used in this work were fabricated by Samsung Electronic Ltd. As a first step in the fabrication process, the gate metal which is a stacked structure of Al and Mo of thickness 150 nm and 50 nm respectively is deposited on top of the glass substrate. In the second step, SiN_x of thickness 430 nm is deposited as the gate insulator. Further, a-Si:H layer of 140 nm is deposited. On top of this intrinsic a-Si layer lies the n+ a-Si layer. Later, n+ layer is etched back in the channel region of the TFT. Source and Drain metal contacts, which are a sandwich structure of Mo/Al/Mo of thickness 50 nm/200 nm/100 nm, are deposited and patterned. A passivating layer of 300 nm SiN_x is deposited and an organic layer of 2.5-3 µm over this passivation layer is deposited.

In addition to the conventional inverted staggered TFTs formed by photolithography, printed TFTs have been developed to avoid the higher cost associated with deposition and lithography steps on large glass substrates. These printed methods hold promise for cheaper and faster production of TFTs for displays. Further, the flexible substrates can be used in conjunction with these printing techniques leading to displays that can conform to various shapes.

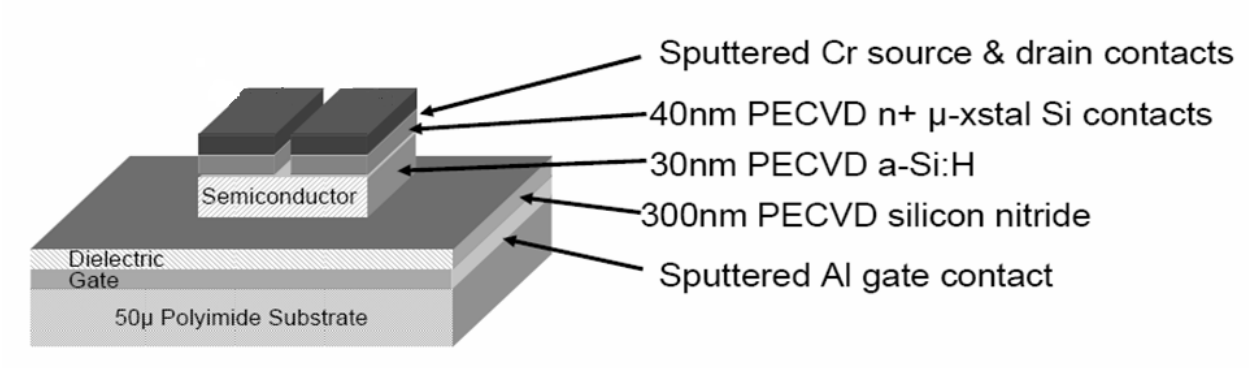

Figure 2-2: Printed Amorphous Silicon Thin film transistor structure fabricated using Roll to Roll process and Self Aligned Imprint Lithography [15]

Recent advances in imprint lithography include resolution of 100 nm and a high throughput of ~ 5 m/min [15]. Further, the PECVD deposition of SiO_x, SiN_x and vacuum deposition of metals has been demonstrated with satisfactory results on flexible substrates. Fig 2-2 shows the structure of a printed a-Si TFT fabricated using the Roll-to-

Roll (R2R) process by HP Research Labs, which is used in this work [15]. The deposition of the stack of materials for the device and the imprint lithography are carried using R2R process. Later, etching is carried out as a batch processing function. Fig 2-2 shows the structure of printed TFT developed by HP Research Labs, based on R2R Self Aligned imprint lithography. As seen in fig 2-2, the structure is inverted staggered structure and the flexible polyimide substrate is used. Al is employed as the gate metal, and the gate insulator is PECVD deposited 300 nm thick layer of Silicon nitride. The channel region is made of 30 nm PECVD deposited a-Si:H layer; and layer of 40 µm N+ layer is deposited and etched so that it remains only in the contact regions. Finally, Cr deposited by sputtering is used as Source and Drain contact metal.

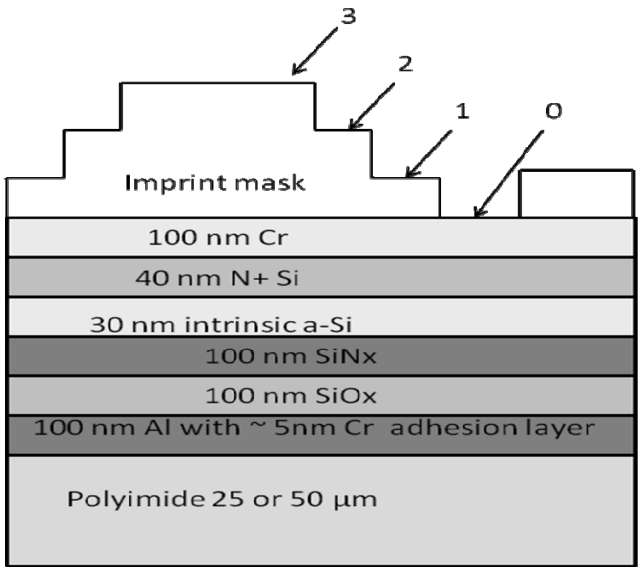

Figure 2-3: The Stack structure for the printed a-Si TFTs, along with the imprint mask shown with 4 levels (marked 0,1,2,3 in the figure) which indicates that 3 material layers beneath the imprint mask – intrinsic a-Si, n+ a-Si and the Cr layers can be pattered using the single mask and multiple etching steps.[16]

The Self Aligned imprint lithography (SAIL) combined with Roll to Roll processing process offers great cost benefits for large scale electronics, since it eliminates the need for photolithography and has very high throughput [16]. In this process, a polyimide substrate with a stack of materials needed for the device is coated with a thin layer of optical adhesive. A polydimethylsiloxane (PDMS) stamp is wrapped around a quartz roller and the stamp patterns the optical adhesive which is then polymerized using UV

light. Fig 2-3 shows the material stack along with the multi-level mask. SAIL uses a single mask to pattern all the layers and solves the layer-to-layer alignment problem by imprinting all the layer information in one step. The information for all the layers is simultaneously imposed using the capability of imprint lithography to create precise layers of different thicknesses. The height information is converted to mask layer information by various incremental etching steps (indicated by 0,1,2 ,3 levels in the fig 2-3) and controlled etching of the polymer mask to remove the lowest height level, while leaving the higher levels. By removing a given multi-level mask level, the stack is uncovered and can be selectively removed by a series of etching steps, giving a transistor. The detailed information about the SAIL process for TFT is provided in [16]

2.2 Current-Voltage measurement

The I-V measurement setup is kept under dark enclosure to avoid photo-effects. The transfer and output I-V characteristics for TFTs with gate lengths of 50 μm and 100 μm are shown in fig. 2-4 and Fig 2-5 respectively. For the output characteristics, the V_{gs} is varied from 4 to 20 V in steps of 2 V each and the drain current is measured for different values of V_{ds}. For the transfer characteristics, the drain current is measured for V_{gs} varying from -10 V to 20 V for V_{ds}=1.1 V, 5.1 V and 10.1 V respectively.

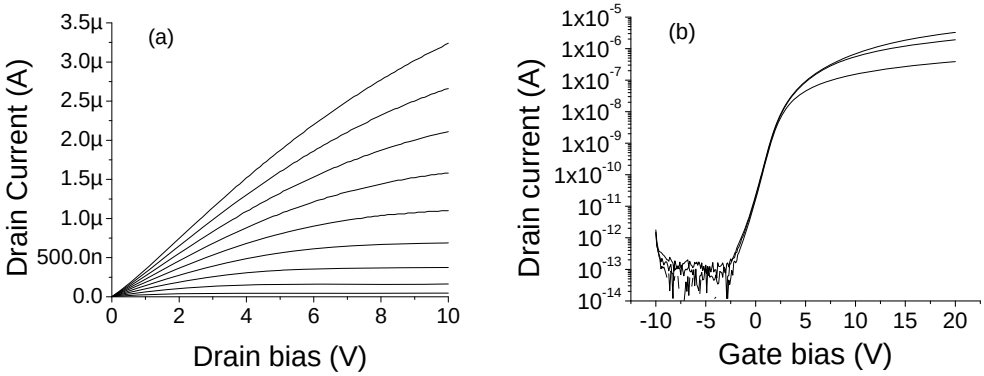

Figure 2-4: Measured (a) output and (b) transfer characteristics for a-Si TFTs with *W*/*L*= 100 μm/50 μm, SiN_x gate insulator of 430 nm (fabricated by Samsung Electronics). For (a), V_{gs} is varied from 4V to 20 V in step of 2V. For (b), V_{ds} is chosen to be 1.1 V, 5.1 V and 10.1 V resp.

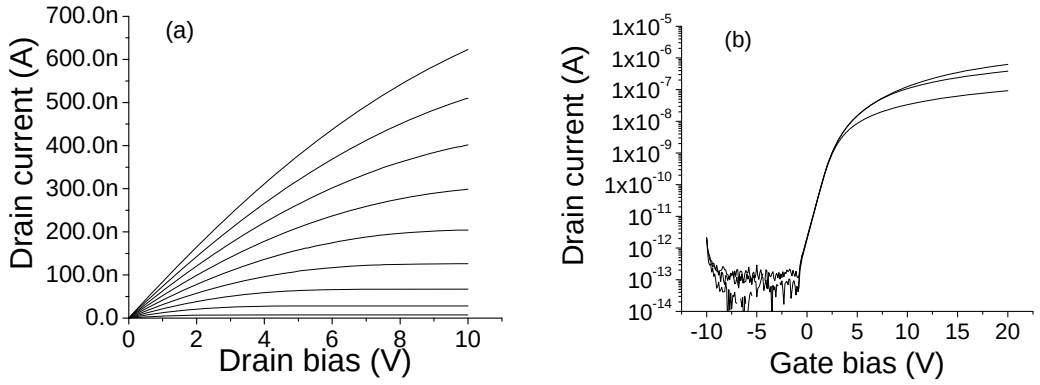

Figure 2-5: Measured (a) output and (b) transfer characteristics for a-Si TFTs with *W/L*= 100 μm/100μm, SiN_x gate insulator of 430 nm (fabricated by Samsung Electronics). For (a), V_{gs} is varied from 4 V to 20 V in step of 2V. For (b), V_{ds} is chosen to be 1.1 V, 5.1 V and 10.1 V resp.

2.3 Capacitance -Voltage measurement

C-V measurements are widely used for determining the doping profile for Schottky barrier diodes, p-n junctions, MOS capacitors and MOSFETs. It can be used to determine the barrier height of Schottky junctions. It has been employed to find the gate oxide thickness in MOS transistors, to find the threshold voltage for MOSFETs, to determine the density of interface trap states at the semiconductor-insulator interface etc [17].

The experimental set-up for the C-V measurement system consists of a probe station, a HP 4284A LCR meter with test probes and a PC with LabView interfaced with the appropriate GPIB cable and interface card. The device under test is placed on the probe station and connected to the LCR meter via the test probes. The LCR meter is interfaced to a computer to collect and process data using a GPIB interface port and LabView. The CV measurement setup is enclosed within a black box in order to eliminate photo-effects. Using the LCR meter, we perform the open circuit and short circuit corrections as a part of the calibration before the measurements. The Open and Short correction functions serve to eliminate measurement errors due to stray parasitic impedance in the measurement setup [18]. During the open circuit correction, the two probes are kept suspended in the air. The precaution to be taken during the short circuit correction is to ensure that the two probes are close by on the same contact pad and the

resistance shown on the LCR meter should be 3-30 ohm (as low as possible). For the capacitance-voltage measurements for conventional TFTs shown in figs.2-6 (a), (b), (c); one probe of the measurement setup was connected to the gate of the device, while the second probe was connected to the source terminal. A small amplitude AC signal superimposed on DC bias is supplied to the gate terminal, while the source terminal is connected to ground and the drain terminal was kept floating.

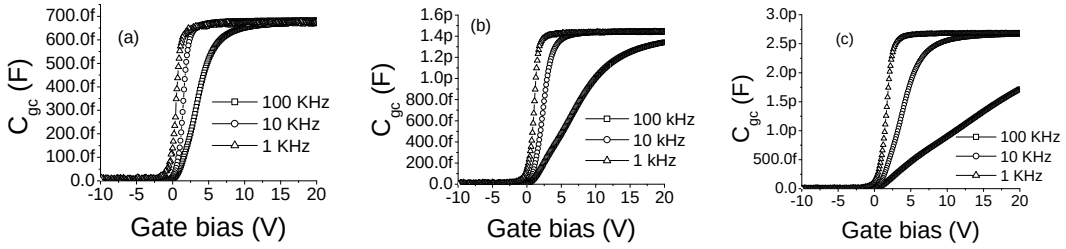

Figure 2-6: Measured capacitance voltage characteristics for a-Si TFTs with (a) *W*/*L*= 100 μm/20 μm, (b) *W*/*L*=100 μm/50 μm, (c) *W*/*L*=100 μm/100 μm. SiN_x gate insulator is 430 nm (Samsung Electronics). Measurement is done with drain terminal left floating and source terminal connected to ground.

For the printed a-Si TFTs, C-V measurements (see fig 2-7 (a) and (b)) were made by connecting the source and drain terminals to the ground, while a small amplitude AC signal mixed with DC bias was applied to the gate of the TFTs.

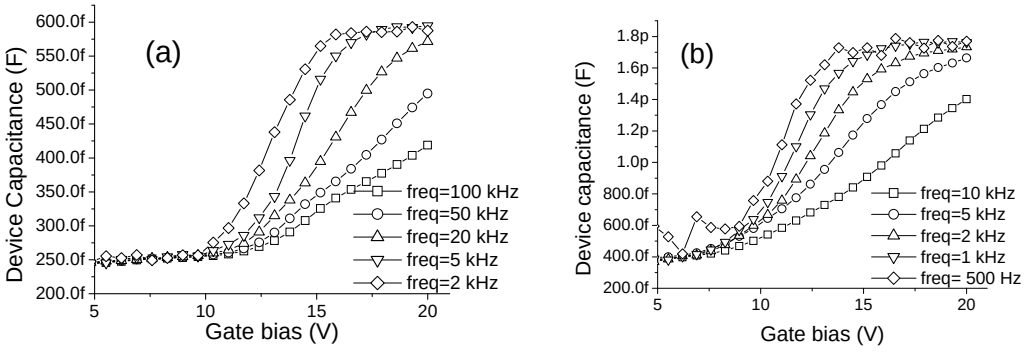

Figure 2-7: Experimental C-V curves for printed a- Si TFT with (a) *L*=20 μm, *W*=100 μm, and (b) *L*=100 μm and *W*= 100 μm. The dielectric stack consists of a SiO_x layer of the thickness of 104 nm, and 207 nm thick SiN_x layer. Both the source and drain terminals are connected to ground

2.4 Experimental errors and limitations

In C-V measurements, the accuracy is limited by the parasitic capacitance associated with the cables used to interface the measurement setup with the PC. Typically, longer length cable leads to less accuracy of measurement. The resistance of the test probes is also likely to cause some limitations in terms of the accuracy of measurement. Errors in C-V measurements can result from an improper short test of the LCR meter during the calibration process. If the short correction displays higher resistance (say, greater than 50 ohm), it is likely to introduce significant error in the measured capacitance curve.

As outlined in [19], C-V measurements suffer from a number of fundamental limitations. For C-V profiling, the maximum depth which can be profiled is limited by the onset of avalanche breakdown. This limit can be significantly extended at the cost of destroying the sample by using an electrolytic Schottky barrier and etching through it while making CV measurements. The second limitation stems from the requirements of depletion approximation, which states that the space region should be completely devoid of mobile charges and the boundary with the neutral region should be abrupt, which are never completely fulfilled.

In general, while measuring the capacitance-voltage of a crystalline MOS transistor, the overlap capacitance at the source and drain should be minimized in order to reduce error. However, for a thin film transistor, the value of the overlap capacitance is significant and needs to be separated to get the gate bias dependent component of the measured capacitance. We describe a method of extracting the overlap capacitance using C-V measurements for transistors of different gate lengths in Chapter 3.

For MOS technologies employing very thin gate oxide [20], the traditional MOS capacitor test structure for capacitance–voltage (C–V) measurement can no longer be used for inversion capacitance extraction because the generation-limited inversion charges are leaked across the thin oxide layer [21]. It may be pointed here that extraction of oxide thickness also depends on accurate knowledge of the inversion capacitance. Consequently, the MOS transistor with source and drain terminals to provide the inversion charges, is commonly used for C-V measurements, wherein the source and drain are connected to ground and small AC signal superimposed on DC bias is applied

to the gate. Further, the measurement of the overlap capacitance is made difficult by the high level of leakage through the ultrathin gate oxide.

All experimental data in this thesis were done by carefully checking the limitations discussed in this section.

3. Models of measured characteristics of amorphous Silicon TFTs

In this Section, we show that we can reasonably reproduce many or even most of the measured characteristics of the Samsung devices using level 16 model of AIM-Spice [27]. The AIM-Spice equations governing the device behavior are presented. The current-voltage and capacitance-voltage modeling of a-Si TFTs have been discussed and ring oscillator modeling is presented.

3.1 Basic Physics of a-Si TFTs (After [28])

Amorphous silicon has large number of localized states in the energy gap. The a-Si TFT is based on the principle of inducing charges at the gate insulator-semiconductor interface by application of electric field, similar to conventional Si MOS transistors. However, due to the disordered nature of amorphous semiconductor material, the low field mobility of a-Si TFT is very small, on the order of 1 cm^2/V-sec.

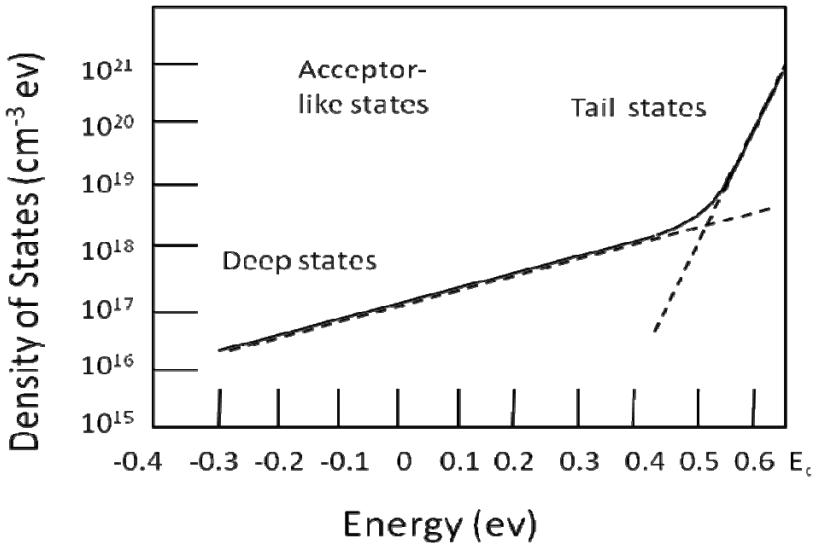

Figure 3-1: Density of states for the acceptor-like states in the energy gap of amorphous silicon [22]

The a-Si TFT has 4 regimes of operation. In addition to the normal below threshold and above threshold regimes as in crystalline Si MOS transistors, there are two additional regimes –transition region and the crystalline like region at high concentration of induced charges. Fig 3-1 shows the distribution of the acceptor like trap states in amorphous Si. For the operation of the a-Si TFT, we focus on the acceptor like states in the upper half of the energy gap at the gate insulator-amorphous Si interface.

In the below threshold regime, almost all the induced charge goes into the deep localized acceptor states of the a-Si. As the gate bias is increased, the Fermi level starts moving towards the conduction band. Once the Fermi level enters the tail states, most of the charge is induced into the states above the Fermi level. In the above threshold regime, most of the charge goes into the tail states, and very less charge goes into the conduction band. As the Fermi level continues to move closer to E_c, the field effect mobility increases with the applied gate bias.

At higher gate biases, the transition regime occurs when all the tail states are almost completely filled and Fermi level is close to E_c. The crystalline regime occurs at very high bias such as 50 to 100 V at which the operation of the a-Si TFT is similar to the conventional Si MOS transistor and the majority of the induced charge goes into the conduction band. We focus on the below threshold and above threshold regimes in this work, since the TFTs for displays mostly operate in these regimes.

3.2 AIM-Spice Level 16 model for TFTs

Spice models for TFTs, accounting for the disordered nature of amorphous semiconductor material, have been included in AIM-Spice. Level 15 was the first model developed for a-Si TFTs. Later, the level 16 model was developed for both amorphous and poly-silicon TFTs [27]. In this work, Level 16 has been used for modeling a-Si TFTs since it is more sophisticated and advanced model; and incorporates the Elmore model for C-V frequency dispersion. These models scale for different TFT dimensions and account for temperature effects. A key feature that distinguishes TFT models from conventional MOS models is the field effect mobility in TFTs in the above threshold regime. The equivalent circuit representation of Level 16 model is depicted in fig 3-2.

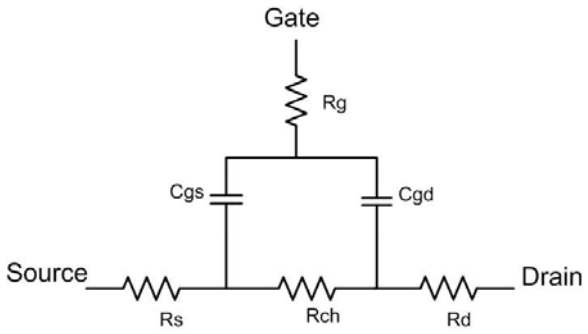

Figure 3-2: Representation of the circuit diagram used in level 16 (After [22])

Current equations-

The above threshold current is given by –

$$I_a = \mu_{FET} C_{ox} \frac{W}{L}\left(V_{gt} V_{ds} - \frac{{V_{ds}}^2}{2\alpha_{sat}} \right) \text{ for } V_{ds}<V_{dsat},\ V_{dsat}=\alpha_{sat} V_{gt} \quad \text{(Eq. 3-1)}$$

$$I_a = \mu_{FET} C_{ox} \frac{W}{L} \frac{{V_{gt}}^2 \alpha_{sat}}{2} \text{ for } V_{ds}\geq V_{dsat},\ V_{dsat}=\alpha_{sat} V_{gt} \quad \text{(Eq. 3-2)}$$

The subthreshold current is given by –

$$I_{sub} = \mu_s C_{ox} \frac{W}{L} (\eta V_{th})^2 \exp\left(\frac{V_{gt}}{\eta V_{th}} \right)\left[1 - \exp\left(-\frac{V_{ds}}{\eta V_{th}} \right) \right] \quad \text{(Eq 3-3)}$$

Capacitance equations-

$$C_{gs} = C_f + \frac{2}{3} * C_{gcs}\left[1 - \left(\frac{V_{dsat} - V_{dse}}{2V_{dsat} - V_{dse}} \right)^2 \right] \quad \text{(Eq 3-4)}$$

$$C_{gd} = C_f + \frac{2}{3} * C_{\text{gcd}}\left[1 - \left(\frac{V_{dsat}}{2V_{dsat} - V_{dse}} \right)^2 \right] \quad \text{(Eq 3-5)}$$

$$C_f = 0.5 * \varepsilon_s * W \quad \text{(Eq. 3-6)}$$

$$V_{dse} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{V_{dsat}} \right)^{mc} \right]^{\frac{1}{mc}}} \quad \text{(Eq. 3-7)}$$

$$C_{\text{gcd}} = \frac{C_{ox}}{1 + \eta_{cd} * \exp\left(\frac{-V_{GT}}{\eta_{cd} * V_{th}} \right)} \quad \text{(Eq. 3-8)}$$

$$C_{gcs} = \frac{Cox}{1 + \eta_{c0} * \exp\left(\frac{-V_{GT}}{\eta_{c0} * Vth} \right)} \quad \text{(Eq. 3-9)}$$

$$\eta_{cd} = \eta_{c0} + \eta_{c00} * V_{dse} \quad \text{(Eq. 3-10)}$$

$$R_g = \frac{{L_g}^2}{Kss \mu_{FET} C_{ox} V_{gte}} \quad \text{(Eq. 3-11)}$$

Table 3-1: Model parameters used in AIM Spice for Thin film Transistors

Parameter	Symbol	Description	Parameter	Symbol	Description
VTO	V_{T0}	Threshold Voltage (V)	RD	R_D	Drain resistance (Ω)
VON	V_{on}	On Voltage (V)	RS	R_S	Source resistance (Ω)
MMU	MMU	Low field mobility exponent	ETA	η	Subthreshold ideality factor
MU0	μ_0	High field mobility (cm^2/Vsec)	ETAC0	η_{c0}	Capacitance subthreshold ideality factor at zero drain bias
MU1	μ_1	Low field mobility parameter (cm^2/Vsec)	ETAC00	η_{c00}	Capacitance subthreshold coefficient of drain bias (1/V)
MUS	μ_s	Subthreshold mobility (cm^2/Vsec)	KSS	k_{ss}	Elmore constant
TOX	t_{ox}	Thin-oxide thickness (m)	DVT	dvt	V_{on} - V_{T0} (V)
CGDO	C_{gdo}	Gate-drain overlap capacitance per meter channel width (F/m)	CGSO	C_{gso}	Gate-source overlap capacitance per meter channel width (F/m)
ASAT	α_{sat}	Proportionality constant of V_{dsat}	MC	mc	Capacitance knee shape parameter
L	L	Gate length of TFT (m)	W	W	Width of TFT (m)

3.3 Device and circuit modeling of a-Si TFTs

We performed modeling of Samsung transistors with width, W=100 μm and lengths varying from 5 μm to 100 μm. Here we present the results for long channel length transistor, in order to separate the contact effects which dominate for short length TFTs. We begin by extracting thickness of the gate insulator (t_{ox}), the oxide capacitance (C_{ox}) and overlap capacitances, C_{gso} and C_{gdo} from C-V measurements. The mobility parameters μ_0, μ_1, MMU were obtained from the I-V results. Finally, simulations on the ring oscillator are performed with the obtained model. In order to extract the gate insulator thickness as well as the overlap capacitance, we plotted the measured maximum capacitance (C_{max}) for different lengths of the TFTs as shown in Fig 3-3. The intercept of this line gives the overlap capacitance and the slope gives us the capacitance per unit length (for the given width of TFT) and can also be used to obtain a verification of the gate oxide thickness through measured data. Such a method of obtaining gate oxide thickness can act as means of overcoming errors, if any, in the calibration during capacitance measurements. For modeling purposes, we treat the gate insulator to be made of SiO_2.

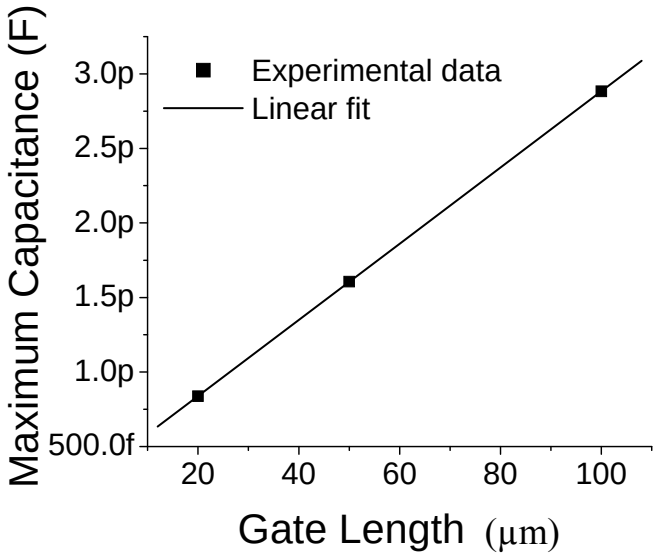

Figure 3-3: Plot of maximum capacitance from measured C-V curves for different gate lengths and the linear fit Y= $3.27*10^{-13}$+ $2.55*10^{-14}$*(X)

Table 3-2: Table of parameters extracted from Fig 3-3

Parameter	Value
tox_real	270.2 nm
C_{gso}	0.164 pF
C_{gdo}	0.164 pF

From fig 3-3, we get the thickness of oxide of the TFT as *tox_real*=27.02*10^{-8} m which is close to expected value from fabrication process. The intercept gives the value of overlap capacitors at the source, C_{gso} and at the drain, C_{gdo} to be 1.64*10^{-13} F each. The threshold voltage V_t was obtained from 1/3rd point of the C-V curves at 10 kHz [23].

3.3.1 I-V model

The contact resistance of TFTs is very high and can dominate the device performance for short channel devices. To find contact resistance, measurement of the resistance for devices of various lengths at low drain bias is needed. The intercept of the plot of resistance against gate length would give the contact resistance. In addition, for short devices, the nonlinearity of the current voltage characteristics at small drain voltage is observed. This non-linearity can be attributed to the contacts. This effect is included in the AIM-Spice modeling by using a diode in series with the TFT. The saturation current (I_{sat}) for the diode is set by the I-V transfer curve corresponding to low values of V_{ds}, which is the region where the non-linearity due to the contacts is observed.

The above threshold current as given in Eq. (3-1) and (3-2), uses field dependent mobility $\mu_{FET,}$ which is defined as the usual crystalline-Si carrier mobility scaled by the ratio of the free carrier density to the induced carrier density. μ_{FET} is found to be empirically given by a power law for lower values of the gate bias and it asymptotically approaches a constant value μ_0, at high-gate biases. It is given by [23]:

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_0} + \frac{1}{\mu_1\left(2*\frac{(V_{gs}-V_t)}{\eta * V_{th}}\right)^{MMU}} \qquad \text{(Eq. 3-12)}$$

The mobility parameters μ_0, μ_1 and *MMU* are extracted from μ_{FET} which can be obtained from the I-V characteristics as outlined in [24]. μ_0 is set from the portion of

transfer curves that corresponds to higher V_{gs} or from the asymptote to the μ_{FET} curve at higher V_{gs} value. μ_1 and MMU are also obtained from μ_{FET} extracted from I-V measurements (refer [24]).

The transfer and output characteristics for inverted-staggered a-Si TFT manufactured by Samsung Electronics Ltd. by conventional methods of lithography and deposition, along with the AIM-Spice simulations are shown in Figures 3-4 and 3-5 resp. It can be observed that the Spice model simulations accurately follow the measured values.

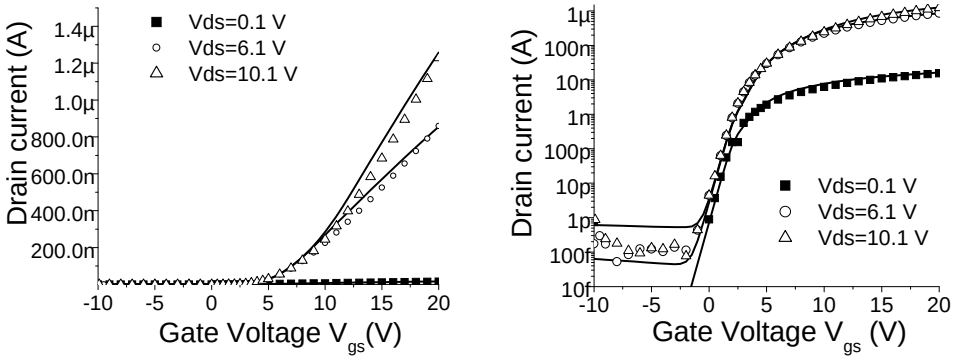

Figure 3-4: Measured and simulated transfer curves for a-Si TFT with *L*=50 µm, *W*=50 µm, shown in both linear and log scales

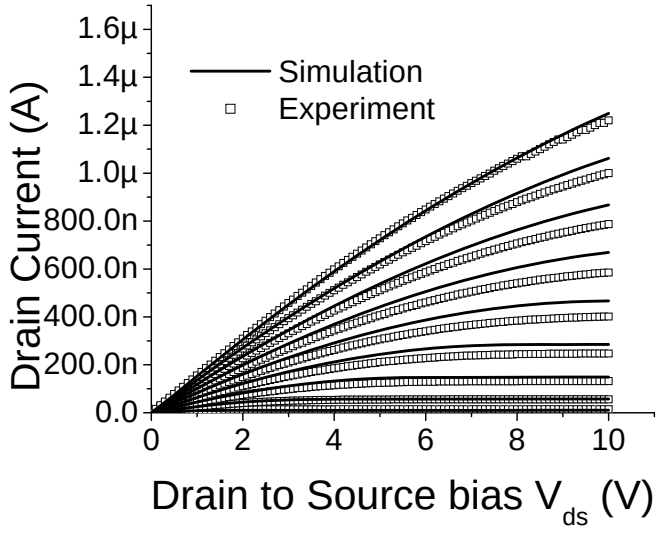

Figure 3-5: Measured and simulated output characteristics for TFT with *L*=50 µm, *W*=50 µm (the gate bias, V_{gs} is varied from 4 V to 20 V in steps of 2V)

Table 3-3: TFT parameters used for I-V modeling in AIM-Spice:

Parameter	Value	Parameter	Value
eta	14	*mc*	3
mmu	0.625	*mu0*	1.15 cm^2/Vsec
mu1	0.25 cm^2/Vsec	*mus*	1.2 cm^2/Vsec
rd	0.55 MΩ	*rs*	0.55 MΩ
tox	$27.02x10^{-8}$ m	*etac*	14
cgso	$0.82x10^{-9}$ F	*cgdo*	$0.82x10^{-9}$ F

3.3.2 C-V model

In chapter 2, it was shown that experimental C-V curves for a-Si TFTs show frequency dispersion**.** Greve and Hay [25] proposed the transmission line model to account for the frequency dispersion observed in TFTs. The equivalent circuit for this distributed R-C line approach is obtained by replacing the TFT channel by a number of subtransistors as given in Figure 3-6. The source and drain overlap capacitances and the source and drain resistors are also included. In this approach, the TFT is replaced by a number of subtransistors, wherein the number of subtransistors used depends on the accuracy needed and is usually more than 10. This model is computationally intensive, since one needs to deal with an increased number of transistors in the simulation circuit.

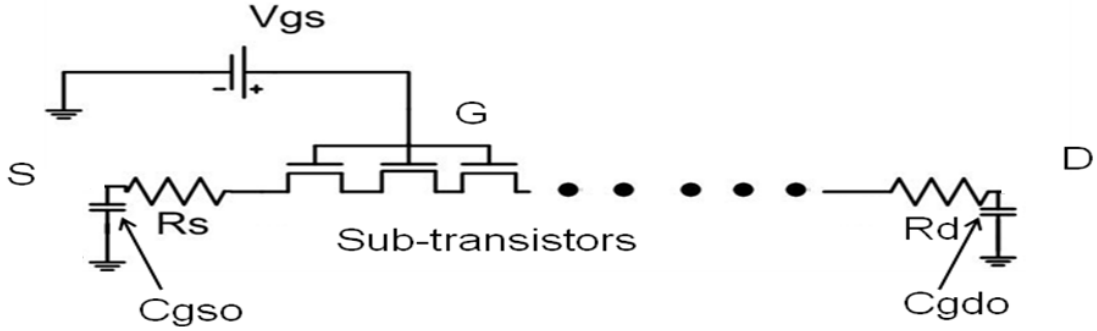

Figure 3-6: Thin film transistor is replaced by a number of sub-transistors for Spice simulation. The overlap capacitors at included at the source and drain ends

The level 16 model in Aim Spice uses the following expressions:

$$C_{gs} = C_f + \frac{2}{3} * C_{gcs}\left[1 - \left(\frac{V_{dsat} - V_{dse}}{2V_{dsat} - V_{dse}}\right)^2\right] \qquad \text{(Eq. 3-13)}$$

$$C_{gd} = C_f + \frac{2}{3} * C_{\text{gcd}} \left[1 - \left(\frac{V_{dsat}}{2V_{dsat} - V_{dse}} \right)^2 \right] \quad \text{(Eq. 3-14)}$$

From the Universal charge control model, C_{gcd} is obtained as –

$$C_{\text{gcd}} = \frac{C_{ox} LW}{1 + 2\exp\left[\frac{-(V_{gs} - V_{ds} - V_t)}{\eta_c V_t} \right]} \quad \text{(Eq 3-15)}$$

where η_c is the capacitance ideality factor which is bias dependent because of the trap states.

It can be seen from equations, that the fringing capacitance term C_f is included in calculation of C_{gs} and C_{gd}. When the TFT is replaced by sub-transistors, we need the fringing capacitance only for the two subtransistors, one each at the source and drain and not for any other sub-transistor. However, it can be seen that the Spice will add the fringing component in all the subtransistors in the circuit. In order to avoid this surplus fringing component inclusion, we have to use effective oxide thickness *tox_eff*. The fringing capacitance is given by $C_f = 0.5 * \varepsilon_s * W$, where $\varepsilon_s = 11.7 * \varepsilon_0$ is the permittivity of amorphous Silicon. Let *tox_real* be the actual thickness of the gate oxide obtained from measurements and *tox_eff* be the effective thickness for use in C-V simulations using sub-transistors in AIM-Spice. If n is the number of sub-transistors used then the following relation holds true-

$$\frac{W * n * L * \varepsilon_i}{tox\_eff} + 2nC_f = \frac{n * W * L * \varepsilon_i}{tox\_real} \quad \text{(Eq. 3-15)}$$

Simplifying, we get

$$tox\_eff = \frac{1}{\frac{1}{tox\_real} - \frac{\varepsilon_s}{\varepsilon_i * L}} \quad \text{(Eq. 3-16)}$$

For simulating the C-V dispersion for TFT of L=50 μm and W=100 μm, we used 20 sub-transistors, each of L=2.5 μm and W=100 μm. For the devices used in this study, we obtained *tox_eff*= 388.2 nm. Fig 3-7 shows a close agreement between the measured capacitance-voltage curves and the C-V curves obtained using sub-transistor approach in AIM-Spice.

Table 3-4: Table of parameters used in AIM-Spice for the sub-transistor model in the simulation results shown in Fig. 3-7

Parameter	Value	Parameter	Value
eta	14	*mc*	3
etac0	25	*mu0*	1.15 cm^2/Vsec
mmu	0.625	*mu1*	0.25 cm^2/Vsec
tox	38.82x10^{-8} m	*mus*	1.2 cm^2/Vsec
dvt	0.1 V	*von*	2.5 V

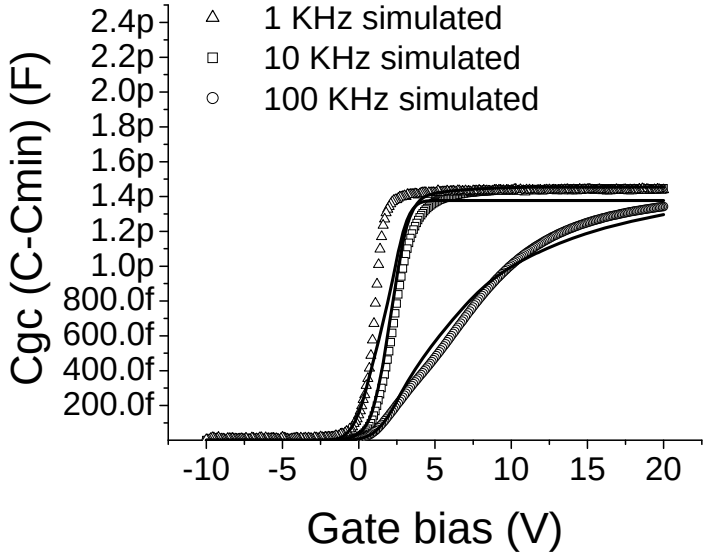

Figure 3-7: The experimental and simulated C-V curves for TFT with *L*=50 µm, *W*=200 µm (device fabricated by Samsung Electronics). Here C_{gc} stands for gate-to-channel capacitance

3.3.3 Ring oscillator modeling

A ring oscillator is commonly used for evaluating technology performance. Further, it is a good circuit for evaluating the AC performance of the TFT model. The inverter stage, with the driver transistor of length, *L*=5 µm and width, *W*=400 µm and the load transistor of length, *L*= 5 µm and width *W*=10 µm, is used in the ring oscillator as shown in fig 3-8. The detailed layout of the ring oscillator is depicted in Fig 3-9. A noise source has to be introduced in the Spice circuit file in order to initiate the oscillations [26]. A

pulse signal source or a piece wise signal source is preferred for representing the noise source in the ring oscillator circuit.

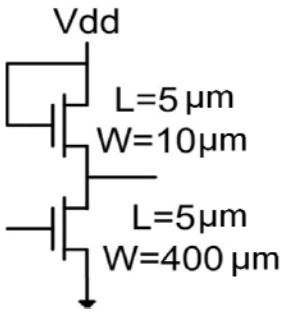

Figure 3-8: Inverter with depletion mode load used as one stage in the ring oscillator

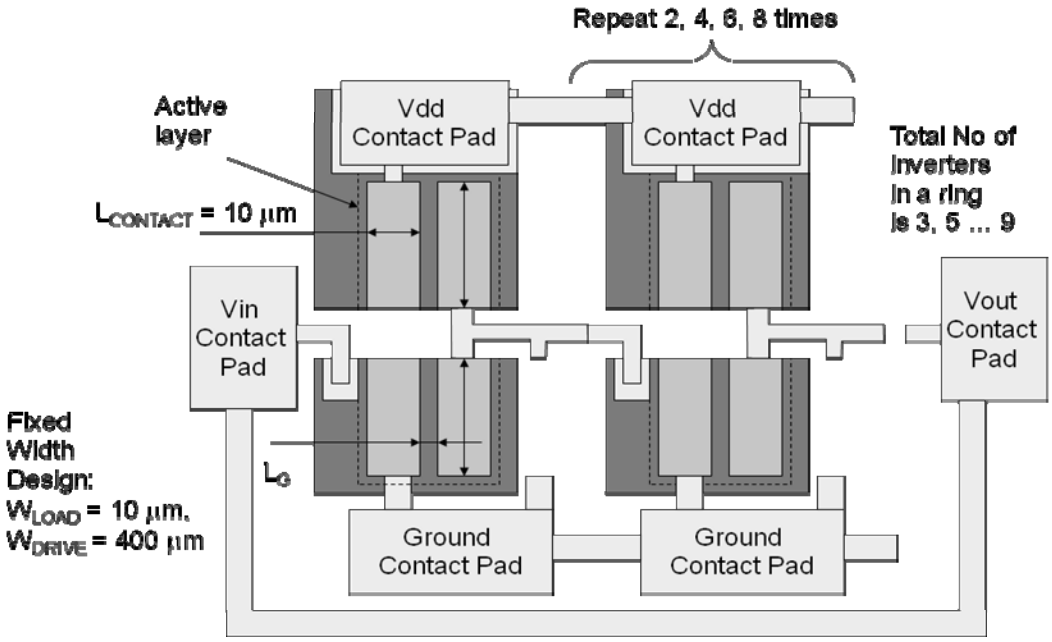

Figure 3-9: Ring oscillator design/layout [50]

Fig. 3-10 shows the frequency of oscillations for ring oscillators of 7, 9 and 11 stages. It can be seen that the simulated values closely agree with measured frequency values for 9 and 11 stage oscillators. The discrepancy with the experimental result for high frequencies, especially for 7 stage oscillator, can be traced to the fact that we did not include the resistance and parasitic capacitance associated with interconnects, which are difficult to model. These interconnect effects exert less influence at lower frequency.

The AIM-Spice circuit file, along with the values of the parameters used in the simulation, is given in Appendix I.

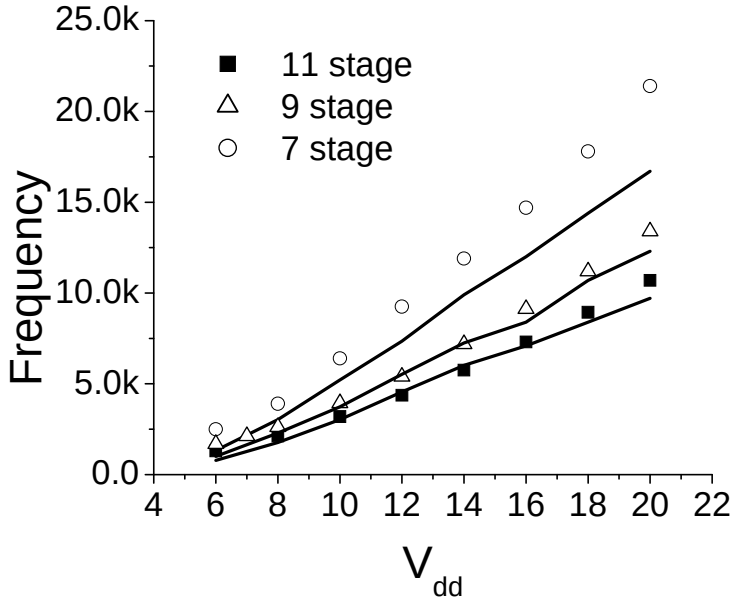

Figure 3-10: Experimental and AIM Spice simulation for frequency of operation of ring oscillators (fabricated by Samsung Electronics) as a function of V_{dd} (in volts). The inverter stage used is shown in Fig 3-8

4. Contact effects and compact capacitance model for printed a-Si TFTs

With the rapid development in fabrication of printed TFTs, it becomes important to have accurate device models for these TFTs. In this chapter, the contact effects for printed TFTs are described and current –voltage modeling is presented in brief. The analytical description of capacitance of FET is presented. A compact capacitance model for printed a-Si TFTs is presented and ring oscillator simulations using the combined Variable Dispersion model (VDM)-Elmore model is performed.

4.1 TFT contact effects

The structure of the contacts of printed TFTs is shown in fig 4-1 along with the energy band diagram. It can be observed that the metal contact is on top of n+ doped layer which is separated from the channel by a thin layer of undoped material. The contact has an n+-i structure and hence, its properties are dependent on the voltage drop across the contact and the bias applied between gate and the channel. This is markedly different from the situation in crystalline semiconductor devices and traditional thin film transistors, and leads to non-ohmic contact behavior in printed TFTs. These nonlinear contact effects can be important and even dominate for short channel devices. The injection of carriers through electrode-active layer interface at the source electrode, limits the current flow leading to non-linear, Schottky-like behavior. In the universal TFT model [30], the contact of a TFT is modeled by a separate contact field effect transistor which accounts for the effect of the contact voltage on the electron density in the semiconductor-dielectric interface under the contact (refer fig 4-2). The diode bridge represents the space charge injection across the undoped semiconductor layer.

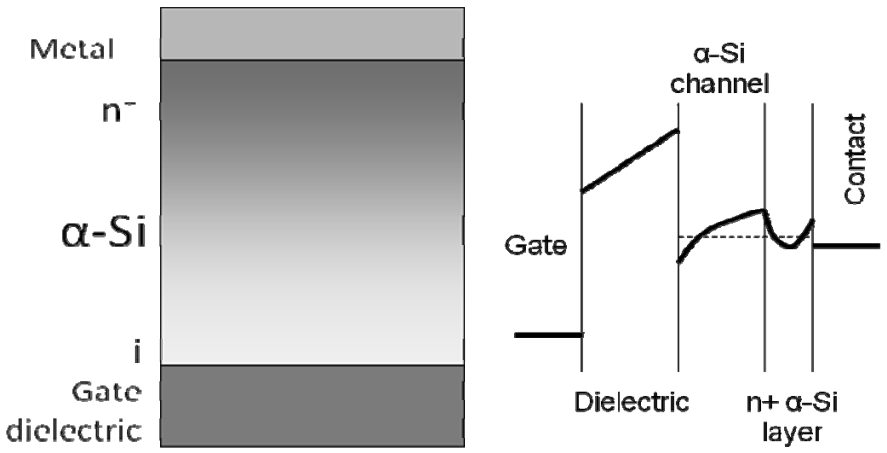

Figure 4-1: Contact structure of a-Si printed TFT, showing the n+ a-Si and the intrinsic a-Si regions at the contact. The band diagram at the contact is also shown [50].

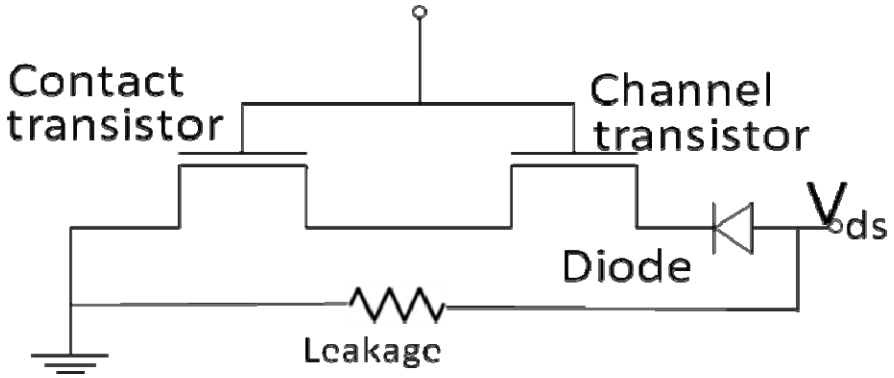

Figure 4-2: Equivalent circuit for the printed TFT, including the contact effects (from [30])

For the best results, the n^+ - i contact structure must have as low thickness of the intrinsic layer as possible. In the real device, however, there are strong technological limitations on the layer thickness. These limitations arise from (a) the real doping profile which is typically diffusion-like and therefore has a transition length, and (b) from the limitation of uniformity and repeatability of the etching process that is used to remove the doped layer in the channel region of a TFT. These limitations also affect the C-V characteristic of the TFT contact.

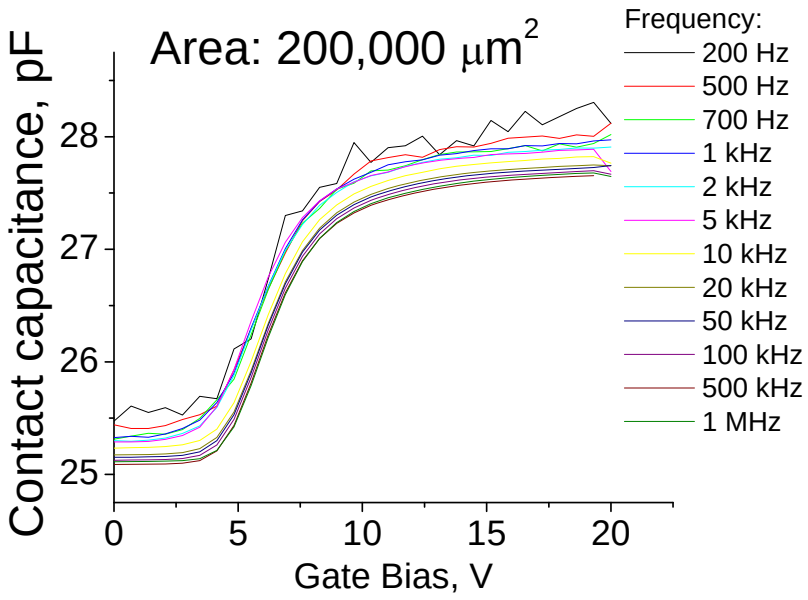

Figure 4-3: C-V measurements for the contact structure for contact with area of $2x10^5$ μm^2

Fig 4-3 shows the measured capacitance at frequencies ranging from 200 HZ to 1 MHz for a contact structure of a very large area (~$2x10^5$ μm^2). The gate dielectric used for this Metal-Oxide-Semiconductor-Metal (MOSM) structure was the same dielectric stack used for the TFT devices. The dielectric stack consists of a SiO_x layer of the thickness of 104 nm, and of a 207 nm thick SiN_x layer. As seen from fig. 4-3, there is negligible frequency dispersion in the contact structure over a wide range of measurement frequencies.

4.2 DC Current-Voltage modeling

In this section, the current voltage modeling for printed thin film transistors is described. The effect of the contact has been included in this I-V modeling. The I-V characteristics were measured at drain bias of 0.3 V, comparable to the typical test AC signal amplitude. Using the simplified RPI TFT model [39, 40], the current equations can be described as follows:

$$I_{SUB} = I_{SAT} \exp\left(\frac{V_G - V_T}{\eta_{C1} V_{th}}\right),$$
$$I_{ABOVE} = gm \cdot V_{GTE},$$
$$V_{GTE} = (V_G - V_T) + \sqrt{(V_G - V_T)^2 + 4(\eta_{C2} V_{th})^2},$$
$$\frac{1}{I_{CHANNEL}} = \frac{1}{I_{SUB}} + \frac{1}{I_{ABOVE}}.$$ (Eq. 4-1)

Here I_{SUB} is the subthreshold current, while I_{ABOVE} refers to the above-threshold current. V_G is the gate bias, V_T is the threshold voltage, V_{th} is thermal voltage, and g_m is the channel transconductance. The values of the parameters used are given in Table 4-1, and comparison with the experimental data is shown in Figure 4-4. There is significant difference between the measured and the simulated I-V curves. This is due to the fact that the measured I-V curves have sub-threshold behavior that cannot be accurately described using a single subthreshold slope. In fact, the subthreshold behavior of the measured I-Vs shows two distinct regions which are straight lines with different slopes.

Table 4-1: Channel-related drain current modeling parameters

Parameter	Value	Unit
V_T	13.5	V
V_{th}	0.026	V
I_{SAT}	20	μA
η_{C1}	20	-
η_{C2}	50	-
gm	156	nS

Next, we divide the subthreshold region into two regions, each of them having a different slope. In the model, we describe this by using two terms for the subthreshold current I_{SUB1} and I_{SUB2}. The physical reason for two different subthreshold slope regions can be traced to the fact that in printed TFTs, the contact plays a role in determining amount of current flow in the channel and contacts can limit the current at low drain bias. Thus, we attribute the two subthreshold currents to different sources – I_{SUB1} can be attributed to device channel and I_{SUB2} can be attributed to device contact. This model is

consistent and follows the reasoning behind the three transistor model suggested recently [30]. It will be shown that this approach gives much better agreement with the measured I-V curves.

The current equations can be written as follows:

$$I_{SUB1} = I_{SAT1} \exp\left(\frac{V_G - V_T}{\eta_{C1} V_{th}}\right),$$

$$I_{SUB2} = I_{SAT2} \exp\left(\frac{V_G - V_T}{\eta_{C2} V_{th}}\right),$$

$$I_{ABOVE} = gm \cdot V_{GTE},$$

$$V_{GTE} = (V_G - V_T) + \sqrt{(V_G - V_T)^2 + 4(\eta_{C2} V_{th})^2}, \qquad \text{(Eq. 4-2)}$$

The total channel current is now given by-

$$\frac{1}{I_{CHANNEL}} = \frac{1}{I_{SUB1}} + \frac{1}{I_{SUB2}} + \frac{1}{I_{ABOVE}}. \qquad \text{(Eq. 4-3)}$$

The results of such an approach are shown in Figure 4-5, with the parameters listed in Table 4-2.

Table 4-2: Drain current modeling parameters

Parameter	Value	Unit
V_T	12.8	V
V_{th}	0.026	V
I_{SAT1}	380	nA
η_{C1}	50	-
I_{SAT2}	900	nA
η_{C2}	28	-
Gm	143	nS

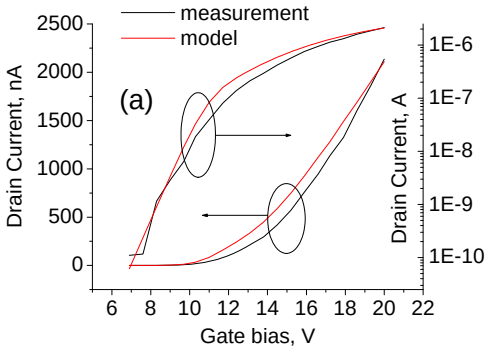

Figure 4-4: Drain current simulation with contact effects excluded, based on the parameters of Table 4-1.

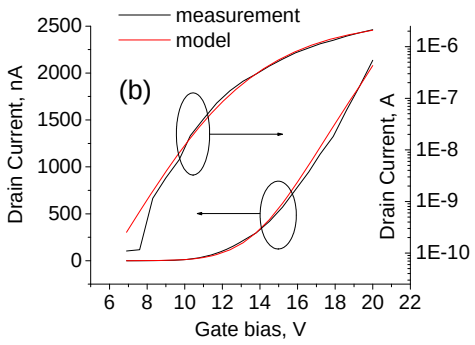

Figure 4-5: Drain current simulation result along with the measured values for the device with 100 µm gate length (Table 4-2).

4.3 Frequency dispersion in printed a-Si TFTs

For the C-V measurements of the TFTs, the source and drain were externally connected to the ground, while 0.1 V amplitude AC signal was applied to the device gate mixed with the DC bias. The C-V characteristics for printed thin film transistors exhibit frequency dispersion. The series resistance of the channel is the major source of frequency dispersion. The transmission line model which accounts for the channel resistance was earlier shown to give good agreement with measured C-V curves for conventional TFTs in chapter 3. The measured capacitance-voltage curves along with the current-voltage characteristics for printed TFTs are shown in fig 4-6.

It can also be observed from fig 4-6, that the capacitance-voltage characteristic exhibits a much lower threshold voltage (V_t) than the DC characteristic of the same device. The threshold voltage is extracted from the 1/3rd point for the C-V curve at 10 kHz as shown in the figure 4-6. The V_{on} voltage is obtained from the I-V curves and is indicated by an arrow in the figure 4-6. The threshold voltage (V_t) is lesser than V_{on} and this can be explained through the concept of gate voltage dependent field effect mobility μ_{FET} [23]. The on current in TFT's is reached when these two conditions are satisfied – (1) the channel is formed and (2) the gate voltage dependent field effect mobility reaches a reasonably high value. The high concentrations of the trapped charge in the channel

near the threshold voltage, where the Fermi energy in the channel crosses the tail states near the conduction band edge, lead to the condition $V_{on}>V_t$.

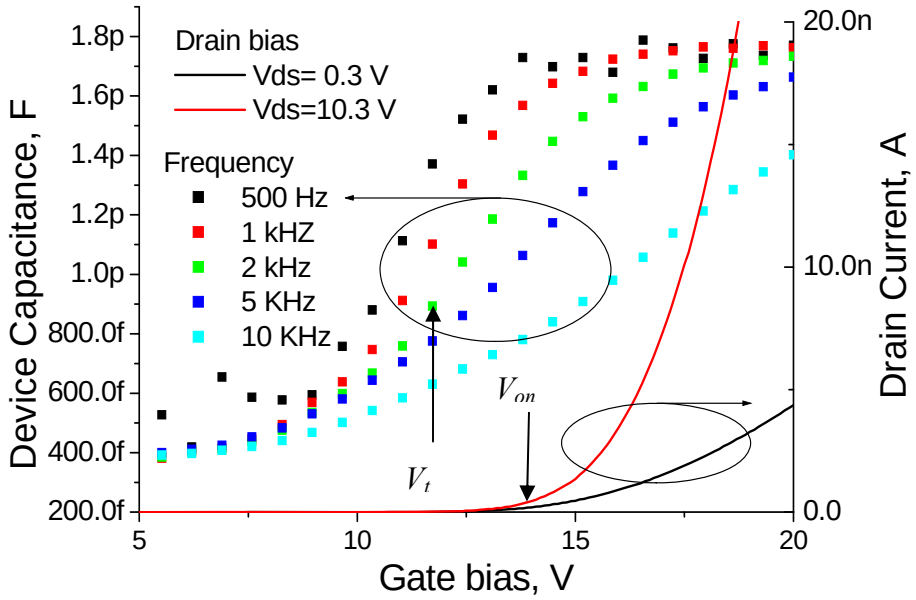

Figure 4-6: Experimental C-V and I-V curves for printed TFT with *L*=20µm, *W*=100 µm. V_t and V_{on} are indicated in arrows in the figure

4.4 Elmore model

The Elmore model represents a non-quasi static approach in which the lowest frequency pole of the RC network is retained [26], leading to reasonably accurate modeling of the charge buildup in the channel. To account for frequency dispersion, we implemented the Elmore model in Aim Spice as a single gate voltage dependent resistance R_g [31] as show in fig 4-7(a):

$$R_g = \frac{L_g^{\,2}}{Kss\mu_{FET}C_{ox}V_{gte}} \qquad \text{(Eq. 4-4)}$$

Figure 4-7 (b) gives the best match to the measured C-V data at zero drain bias that can be obtained using the Elmore model in AIM-Spice level 16. It can be seen that the Elmore model follows the general trend of the dispersion, but fails to model the

dispersion completely. In particular, the Elmore model is incapable of reproducing the threshold voltage shift observed in the experimental C-V data at lower frequencies, as indicated by arrows in fig 4-7 (b).

$$\tau_1 = \frac{L_g^{\,2}}{\mu_{FET} * V_{eff}} \qquad \text{(Eq. 4-5)}$$

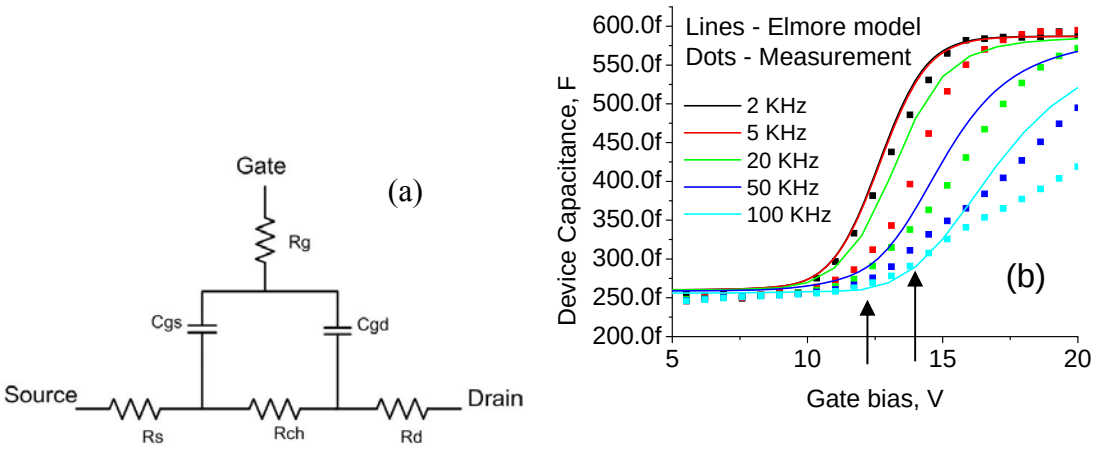

Figure 4-7: (a) Single resistor Elmore model for a-Si TFTs [31] and (b) C-V simulation results for Elmore model implemented in Aim-Spice, with *kss*=6

The important point to note is that the Elmore model considers that the frequency dispersion is only due to the length dependent time constant (of the order of τ_1 given in Eq. (4-5), where the μ_{FET} is the field effect mobility and V_{eff} is the effective voltage that depends on the gate and drain biases). This channel length transit time leads to gate length dependent frequency dispersion

4.5 Analytical description of capacitance in FET

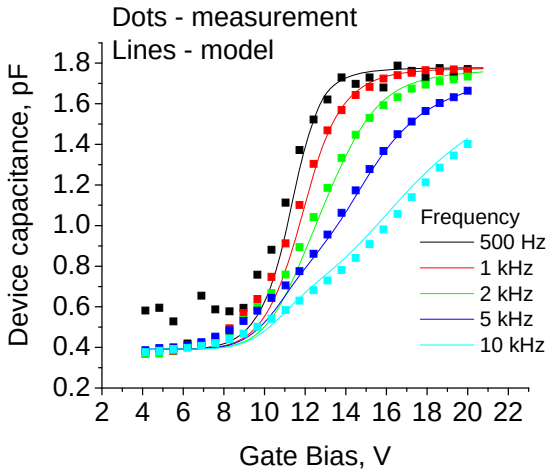

Figure 4-8: Simulated and measured C-V data. The simulated data is obtained using 100 stage distributed line model and flat or constant capacitance

Table 4-3: Parameters used for plots in Figs 4-8 and 4-9

Parameter	Value
eta	50
W	100 μm
L	100 μm
V_{th} (threshold voltage)	11.5 V
Overlap capacitance/unit area	14 nF/cm^2

The frequency dispersion in TFTs can be accounted using the distributed channel model. Fig 4-8 shows the simulated and measured C-V curves using distributed channel model. The channel was replaced by 100 stage transmission line and the resistance data from Table 4-2 is used.

In this section, we present the analytical description of the capacitance of the FET [38]. Let $U(x,t) = V_G - V_{ch}(x,t)$ denote the local gate-to-channel potential. We consider threshold voltage to be zero (alternately, V_t is subtracted from U). Let n_S be the sheet carrier density. We consider that n_S is a function of U and can be expressed in general form by $n_S = f(U)$ and μ is the mobility and R_{SH} is the channel sheet resistance given by:

$$R_{SH} = \frac{1}{q\mu n_S} \qquad \text{(Eq. 4-6)}$$

Let C_{ch} denote the channel capacitance. Unlike the gate dielectric capacitance, for channel capacitance, we have

$$C_{ch} = q\frac{dn_S}{dU} = qf'(U) \qquad \text{(Eq. 4-7)}$$

The derivative with respect to voltage for function f is represented by $f'(U)$. For the linearization purposes, we introduce small voltage disturbance, δU: $U(x,t) = U_0 + \delta U(x,t)$, where U_0 is constant, equal to steady state gate to source voltage. We assume that the drain bias is zero.

The telegraph equations for transmission line can be derived as follows:

$$\frac{dU}{dx} = -R \cdot I\,, \qquad \text{(Eq. 4-8)}$$

where elementary resistance $R = R_{SH}/W$ and I is the channel current (W is the channel width), and

$$\frac{dI}{dx} = -i\omega C_{ch} \cdot U\,. \qquad \text{(Eq. 4-9)}$$

Note that in Eq. (4-9), the real bias-dependent capacitance (and not the geometric capacitance), that links charge transport to the applied bias, is used.

Combining (4-8) and (4-9), we get:

$$\frac{d\left(-\frac{1}{R}\cdot\frac{dU}{dx}\right)}{dx} = -i\omega C_{ch} \cdot U \qquad \text{(Eq. 4-10)}$$

Converting all the variables in eq.(4-10) into transport parameters:

$$\frac{d\left(q\mu \cdot f(U)\cdot\frac{dU}{dx}\right)}{dx} = -i\omega \cdot qf'(U)\cdot U \qquad \text{(Eq. 4-11)}$$

Linearizing (4-11) with respect to δU and using for $f(U)$

$$f(U) = f(U_0 + \delta U) \approx f(U_0) + f'(U_0)\cdot\delta U\,, \qquad \text{(Eq. 4-12)}$$

$$\mu \cdot f(U_0)\cdot\frac{d^2U}{dx^2} = i\omega \cdot f'(U)\cdot U, \quad or \quad \frac{d^2U}{dx^2} = \left(\frac{i\omega \cdot f'(U_0)}{\mu \cdot f(U_0)}\right)\cdot U \qquad \text{(Eq. 4-13)}$$

The solution to (4-13) will, therefore, be based on the propagation constant in a form

$$\gamma_{TELEGRAPH} = \sqrt{\frac{-i\omega \cdot f'(U_0)}{\mu \cdot f(U_0)}} \qquad \text{(Eq. 4-14)}$$

We now consider the continuity equation:

$$\frac{\partial n_S}{\partial t} + \frac{\partial (n_S v)}{\partial x} = 0\,, \qquad \text{(Eq. 4-15)}$$

where v is the electron velocity which is given by:

$$v = -\mu \frac{\partial U}{\partial x}\,. \qquad \text{(Eq. 4-16)}$$

Substituting the linearization of the sheet carrier concentration given by (4-12), Eq. (4-15) turns into the following:

$$\frac{\partial (f'(U_0) \cdot \delta U)}{\partial t} - \frac{\partial \left(f(U_0) \cdot \mu \cdot \frac{\partial \delta U}{\partial x} \right)}{\partial x} = 0\,. \qquad \text{(Eq. 4-17)}$$

The propagation constant for the Eq. (4-17) can be expressed as:

$$\gamma_{CONTINUITY} = \sqrt{\frac{-i\omega \cdot f'(U_0)}{\mu \cdot f(U_0)}} \qquad \text{(Eq. 4-18)}$$

This is exactly the same as propagation constant ($\gamma_{TELEGRAPH}$) for Eq. (4-13), given by Eq. (4-14).

Next, we consider the Universal Charge Control Model (UCCM) expression for n_S (including the threshold voltage)[26]

$$n_S = n_0 \log\left(1 + \exp\left(\frac{U}{\eta V_T}\right)\right), \qquad \text{(Eq. 4-19)}$$

where V_T is the thermal voltage and η is the ideality factor.

Now the expressions for f, f' and propagation constant are given by:

$$f(U_0) = n_0 \log\left(1 + \exp\left(\frac{U_0}{\eta V_T}\right)\right), \qquad \text{(Eq. 4-20)}$$

$$f'(U_0) = n_0 \frac{\exp\left(\frac{U_0}{\eta V_T}\right)/\eta V_T}{\left(1+\exp\left(\frac{U_0}{\eta V_T}\right)\right)} = \frac{n_0}{\eta V_T \cdot \left(1+\exp\left(-\frac{U_0}{\eta V_T}\right)\right)} \quad \text{(Eq. 4-21)}$$

and

$$\gamma = \sqrt{\frac{-i\omega}{\mu \cdot \eta V_T \cdot \left(1+\exp\left(-\frac{U_0}{\eta V_T}\right)\right) \cdot \ln\left(1+\exp\left(\frac{U_0}{\eta V_T}\right)\right)}} \quad \text{(Eq. 4-22)}$$

The impedance can now be stated as:

$$Z = Z_0 \coth(\gamma L),\ Z_0 = \frac{1}{W}\sqrt{\frac{R_{SH}}{j * \omega C}} \quad \text{(Eq. 4-23)}$$

where $R_{SH} = \frac{1}{q\mu n_s} = \frac{1}{q\mu n_o \ln\left[1+\exp\left(\frac{U_o}{\eta V_T}\right)\right]} = \frac{1}{\mu C \eta V_T \ln\left[1+\exp\left(\frac{U_0}{\eta V_T}\right)\right]}$ (Eq. 4-24)

This gives the capacitance as:

$$C(\omega) = -\frac{1}{\omega \,\mathrm{Im}(Z)} \quad \text{(Eq. 4-25)}$$

Using this compact model, C-V simulations were performed and the result is shown in Fig 4-9. It can be observed that the result is very similar to the result from distributed channel model results shown in Fig 4-8.

The above derivation works in all regimes of transistor operation and we showed that the derivation for propagation constant obtained using the continuity equations is similar to the telegrapher's solution for transmission lines. In addition, during operation near the threshold voltage, the escaping of the electrons from the localized states might take considerable time, implying that AC variation of density of electrons with time occurs with delay as compared to the variation of gate voltage. One can show that in this case the capacitance is mostly determined by thermo-activated escape of electrons from localized states to conduction band. The rate of such escape exponentially decreases with

decreasing the gate-to-channel swing. This may explain sharp decrease of capacitance observed deep in subthreshold regime [38].

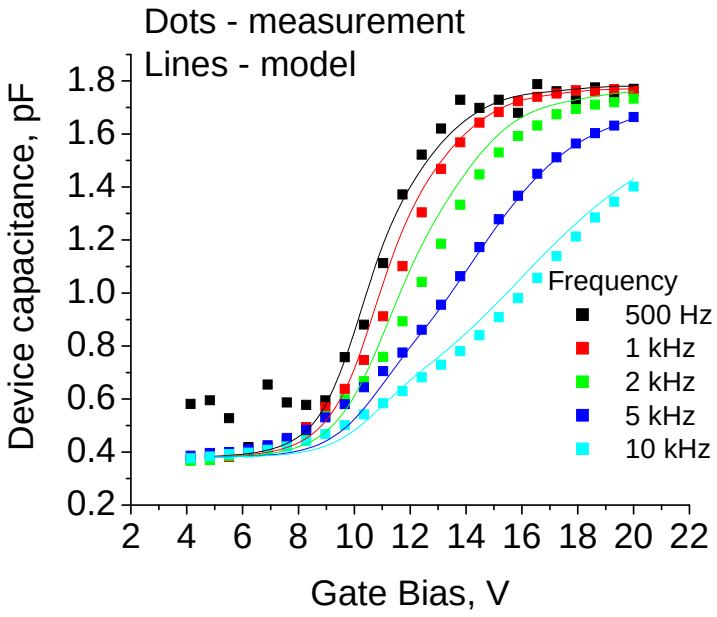

Figure 4-9: C-V simulations using the compact model obtained using Eq. 4-25 and parameters from Table 4-3

4.6 Variable Dispersion Model

If we consider the threshold voltage to be at 1/3rd of the C-V curves, then one can consider shift in the threshold voltage (as seen in Fig 4-7 (b)). Here we present a model for the frequency dispersion that is based on threshold voltage shift. In order to model the gate length independent dispersion in printed a-Si TFTs, we implemented a new level 33 in AIM-Spice. In this level, we introduced the Variable Dispersion Model (VDM) [37]. In VDM, the frequency-dependent carrier temperature is related to effective electron energy redistribution time τ_e as follows [37]:

$$V_{th\_effective} = \frac{kT_{effective}}{q} = \frac{kT}{q}\left(1+\frac{f}{f_e}\right)^{mf}, \quad f_e = \frac{1}{\tau_e} \qquad \text{(Eq. 4-15)}$$

Here, $V_{th\_effective}$ is effective thermal voltage, and mf is the fitting parameter responsible for the frequency dependence sharpness, and f is the frequency of operation.

For our measured C-V data, we chose f_e to be 2 kHz to get optimal match using the combined Elmore-Variable dispersion (VDM) model. From Figure 4-10, it can be observed that the combined Elmore- VDM model accurately describes the frequency dispersion observed in printed TFTs. The agreement with the experiment is much better than for the Elmore model.

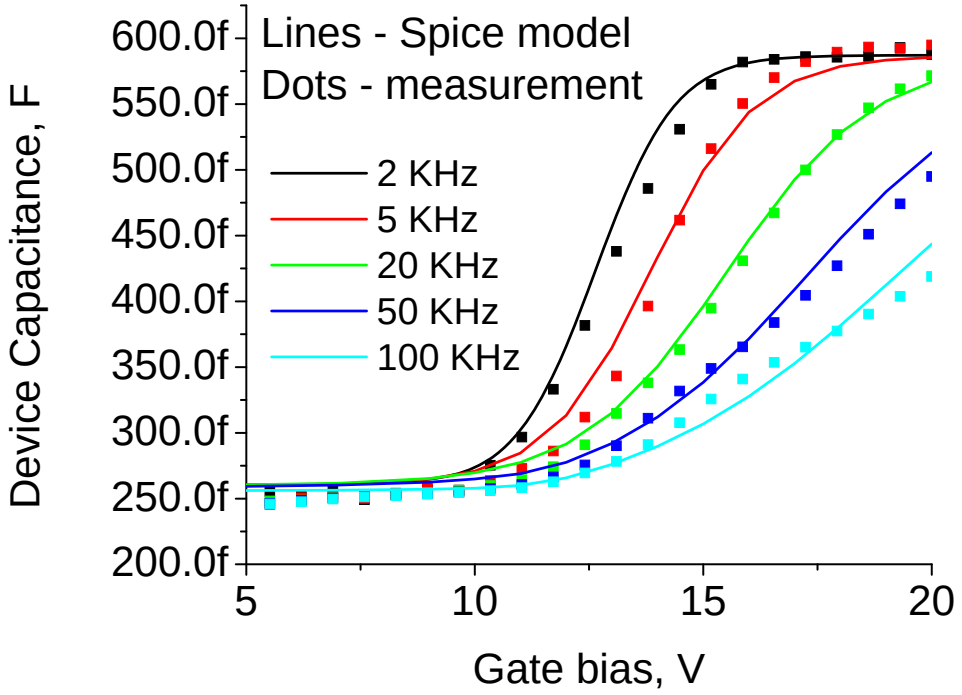

Figure 4-10: C-V simulations results for the combined Elmore-Variable Dispersion model in AIM-Spice showing match with measured data, using *mf*=0.3 and *kss*=6

Table 4-4: AIM-Spice parameters used in the Elmore-VDM model for Fig 4-10

Parameter	Value	Parameter	Value
eta	37	*etac*	30
mmu	1	*mu0*	10 cm^2/Vsec
mu1	0.0022 cm^2/Vsec	*mus*	0.001 cm^2/Vsec
tox	211.4 nm	*Von*	12.75 V
dvt	2.75 V	*mc*	3
kss	6	*mf*	0.3

4.7 Circuit simulation results

In order to see the effect of the new Variable Dispersion model on circuit simulation, we performed transient simulations of ring oscillators using Aim Spice. Noise source was included in the AIM Spice circuit file in order to initiate the oscillations. Initially, we performed simulations in Level 16 without Elmore model to get frequency of operation, excluding any dispersion effect. Next, simulations with Elmore model in Level 16 were performed to obtain frequency of oscillation of the circuit, in order to see the effect of only dispersion related to channel length transit time. The frequency of oscillations of the ring oscillator with Elmore model was substituted as f in the expression for $V_{th\_effective}$ in the Variable Dispersion model Eq.(4-15). Subsequently, Aim Spice simulation was carried with the combined Elmore-Variable Dispersion model (level 33) and this new frequency is plugged back as f in Eq.(4-15) as an iterative process. Typically, a couple of iterations suffice for convergence.

Aim Spice simulations for 7 stage and 11 stage ring oscillators are shown in fig. 4-11. It can be clearly seen that the results for the three models; the level 16 without Elmore, the Elmore model and the combined Elmore-Variable dispersion model, are significantly different from each other. These simulation results indicate that the energy relaxation time constant associated with printed TFTs is likely to exert considerable effect on the circuit performance at even frequency of several kHz. Consequently, for printed amorphous semiconductor devices, considering the dispersion arising from time constant of electron energy redistribution seems important based on the simulation results [37].

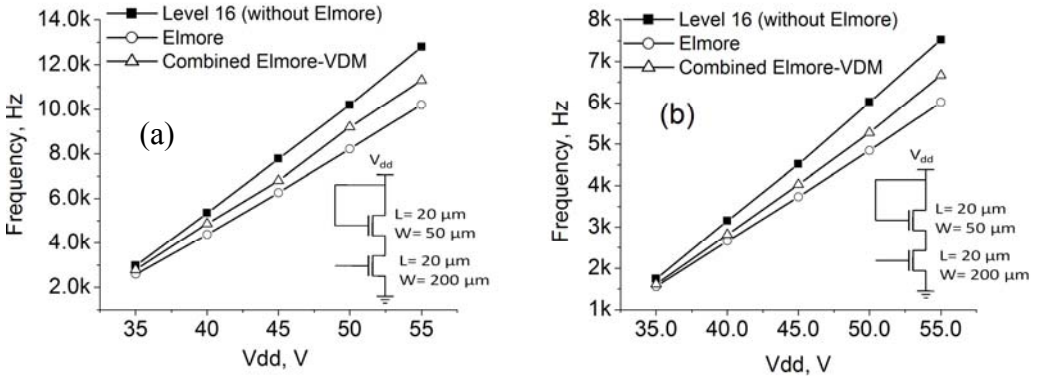

Figure 4-11: Frequency of oscillation for (a) 7 stage ring oscillator and (b) 11 stage ring oscillator using different models in AIM-Spice (inset shows the schematic of inverter stage)

5. Dynamic thermal effects in thin film transistor displays

In this chapter, the thermal circuit for dynamic heating effects in TFTs in large sized displays is presented. TFTs in the active matrix panel are operated in pulsed mode and hence the static analysis of self heating does not provide much insight. It is important to study the dynamic self heating in the TFTs during the actual operation of the display.

5.1 Self-heating in TFTs

The self-heating analysis is very important for a-Si thin film transistors. The a-Si:H channel layer has a very poor thermal conductivity (1.1W/m K) [47]. The substrate, typically glass, is also a good thermal insulator. As a result, the heat removal is worse as compared to crystalline Silicon technology and hence, results in higher temperatures due to self-heating in a-Si TFTs. Due to self heating, the TFT operation is affected and there can be adverse effects on the reliability of the devices. It can be seen from Fig 5-1 that the drain current increases with temperature rise. Generally, an increase of the field effect mobility (μ_{FET}) and a decrease of the threshold voltage (V_t) are observed with increase in temperature. A study of self-heating effects during static operation of TFTs has been presented in [39]. Here static operation refers to DC operation of the TFT.

5.2 Dynamic thermal simulations for TFT LCD panels

The self-heating issue becomes more important as size of the LCD panel increases. While static analysis of self heating effects can be helpful, it is more important to get an idea of the self heating effects during dynamic operation of the TFTs in the LCD panels for displays. Each TFT is switched on for short period of time and thus, one could say that operation is in “pulsed” mode. It may be mentioned that it is not possible to measure the temperature of a TFT device during actual operation, since the TFT is placed between two glass panels and the liquid crystal (refer fig 5-2). One can measure the temperature of the glass panels. However, since the glass used in the panels is a bad conductor of heat, the actual temperature of the TFT during operation may be quite higher than the temperature of the glass panel. A study of dynamic self heating effects can help us get an estimate the actual temperature of the TFTs during operation. It can enable detailed study on reliability issues, and can lead to better and more intelligent

designs of LCD panels that could help to reduce the self-heating effects. The accurate knowledge of the TFT temperature during the operation is important for accurate electrical simulations of the TFT circuits used in displays.

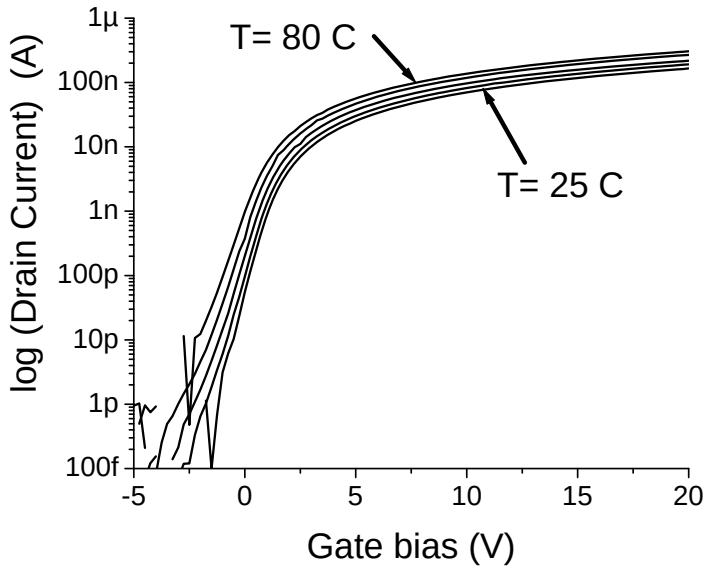

Figure 5-1: Measured drain current plotted at temperatures of 25 C, 35 C, 50 C, 65 C and 80 C for varying gate bias for a-Si TFT of *W/L*= 100 µm/50 µm (fabricated by Samsung Electronics Ltd.). The drain current increases with increase in temperature

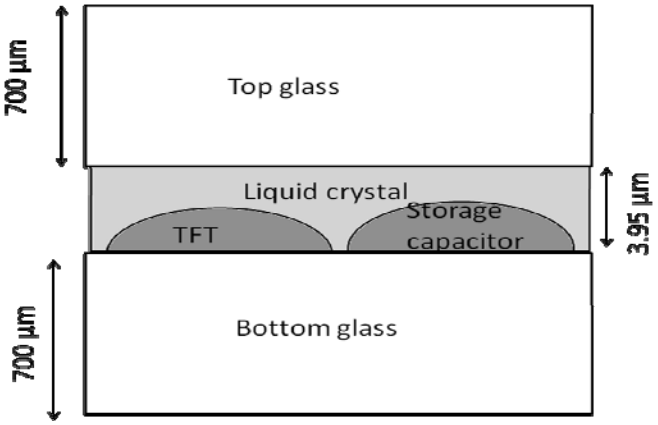

Figure 5-2: Schematic diagram (not to scale) showing the structure for a single pixel in AMLCD panel (Samsung Electronic Ltd.). The top and the bottom glass panels are of 700 µm thickness and the Liquid crystal is 3.95 µm thick.

Here we present the first order dynamic thermal simulations. The most precise method for the study of heat transfer relies on solving the differential heat flow equations. This approach is not feasible since it involves complicated boundary conditions for electronic devices and is very computationally intensive if such a study is pursued for arrays of TFTs in a large sized display. In this work, we study the roles that all the components of device structure and the interconnect network on the heat transfer process under the operating conditions in a large sized LCD display. We present simplified dynamic thermal circuit for modeling dynamic self-heating effects in TFTs.

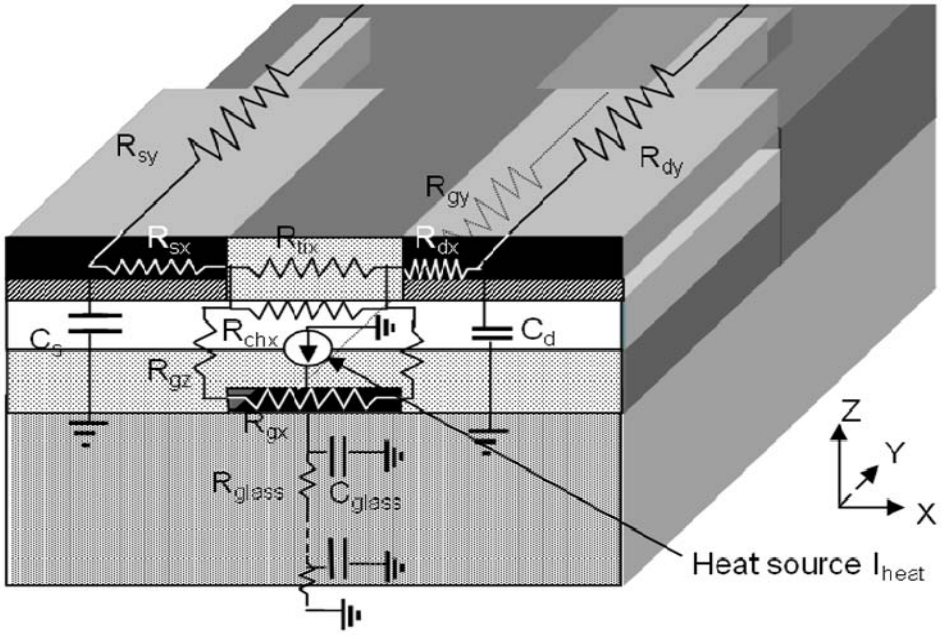

Figure 5-3: Physical model of TFT with equivalent thermal resistances and capacitances shown. Note that only the TFT and the bottom glass substrate are shown here. The top glass and the liquid crystal are not shown. Note that the resistances are designated this way: "g" represents gate, "s", source; "d", drain; "ti" top insulator; the last letter of the subscripts represents the direction of the heat flow along which the resistance is accounted. [40]

The structure of the a-Si TFT fabricated by Samsung Electronics along with the fabrication details have been provided in Chapter 2. Fig 5-3 shows the physical structure of the TFT on glass substrate with equivalent resistances and capacitances associated with the TFT and the bottom glass substrate. The thermal conductivities of the materials are listed in Table 5-1. Here we assumed that all thermal conductivities are temperature-independent. In this model, heat radiation is neglected.

Table 5-1: Thermal conductivity of materials

Material	Thermal conductivity (W/m·K)
Glass (substrate)	0.81[46]
Al/Mo (gate, drain/source metal contact)	250/138 [49]
a-Si:H (channel active layer)	1.1[47]
Si_3N_4 (gate insulator, top insulator)	16.8[48]

The power dissipated (=*I* * *V*) in the TFT is the heat source and is represented by a current source in the equivalent thermal circuit, while temperature is equivalent to voltage in the thermal circuit. The approximate power pulse, which is included as current source in the thermal circuit, is shown in figure 5-4. More accurate power pulse obtained from electrical simulation of the entire display panel can lead to better thermal simulation.

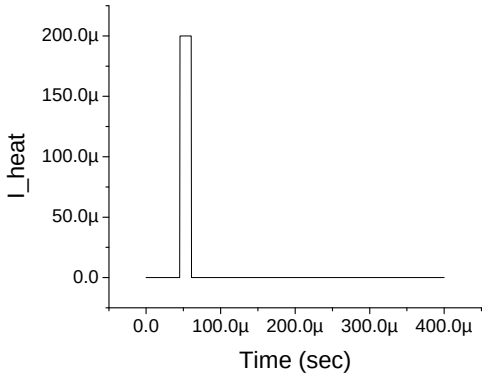

Figure 5-4: Power pulse is included in thermal circuit as current source. The pulse "on" duration is $15x10^{-6}$ sec and the period is 0.4 msec

As a first step, we tried to model the propagation of heat through the glass substrate. Here we consider the TFT to be on a glass substrate and do not consider any of the following – interconnects and the liquid crystal. Under these considerations, the heat propagates from the TFTs through the glass substrate. The heat does not reach the bottom of the glass instantaneously. Such a behavior of slow transfer of heat can be modeled in terms of electrical circuit by using a transmission line. Fig 5-5 shows the transmission line model for heat propagation through the glass substrate. We compared

this circuit with the previous work [45] for GaN Schottky diode and this approach was found to be in close agreement with analytical solution for the GaN Schottky diode [45]. As an initial approximation, the R_{glass} and C_{glass} are calculated by just considering the area of glass beneath the actual TFT device, without considering the spreading effects. The glass substrate was divided into 100 equal layers and equivalent thermal resistance R_{glass} and C_{glass} was used for each layer. This gives a 100 stage transmission line as shown in fig 5-5.

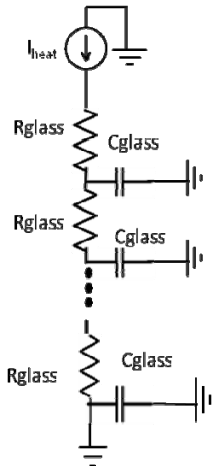

Figure 5-5: Transmission line representation for the heat propagation through the bottom glass panel. The glass substrate was divided into 100 parts and the equivalent thermal circuit is 100 stage transmission line.

5.3 Equivalent thermal circuit

We established the lumped thermal equivalent circuit accounting for the quasi-3D heat flow through the TFT array, which is shown in Figure 5-6.

Using the equation for the thermal resistance of heat conduction:

$$R_k = \frac{L}{Ak} \qquad \text{(Eq. 5-1)}$$

where R_k is the thermal resistance, L is the distance along which the heat is flowing, A is the cross sectional area of the heat conduction and k is the thermal conductivity.

For the thermal capacitance, we used the formula:

$$Cap = m * c_h \qquad \text{(Eq. 5-2)}$$

where *Cap* is the thermal capacitance, *m* is mass of the substance and c_h is the specific heat capacity.

For the calculating the capacitance offered by the glass substrate, only the portion of the glass underneath the device was considered. The values of the various components in the thermal circuit, along with the formulae and approximations used are given in Table 5-2. The values of the components are based on actual TFT devices arranged in a 32 inch LCD display manufactured by Samsung Electronics Ltd.

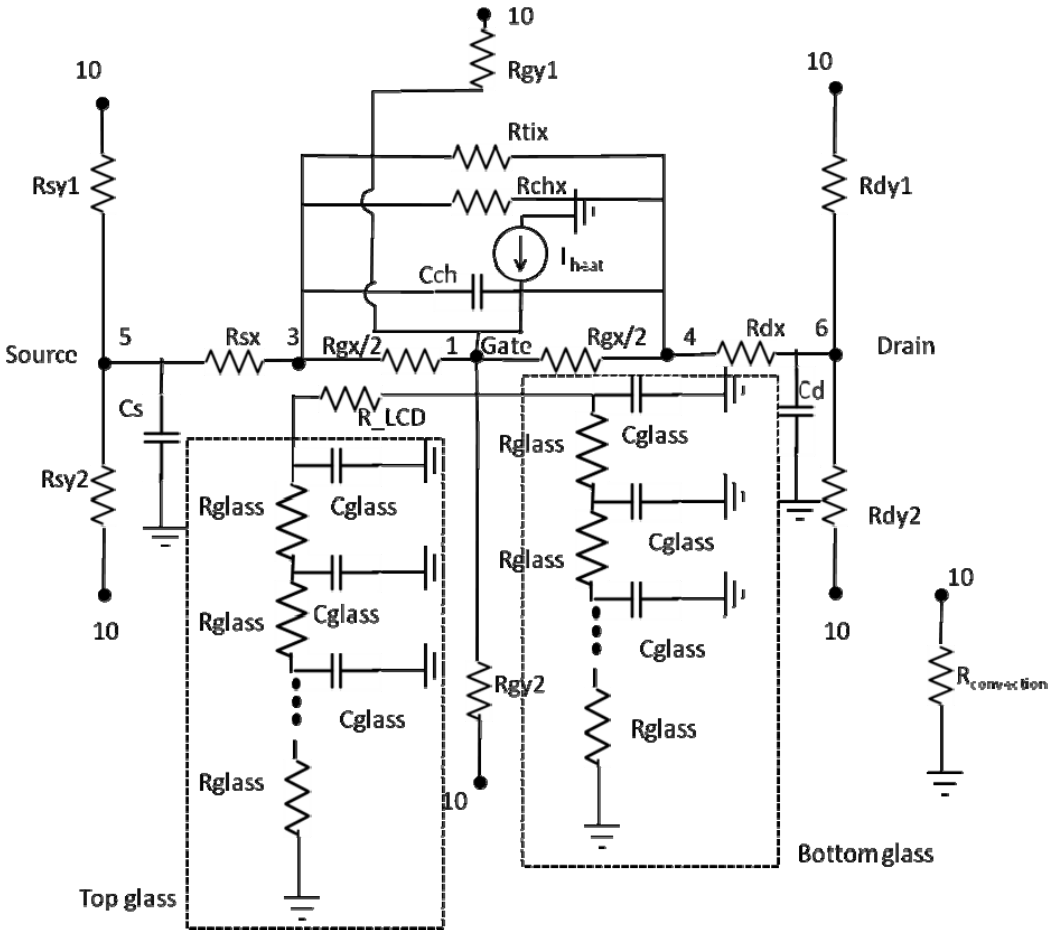

Figure 5-6: Dynamic heat circuit, including interconnect thermal resistors and the transmission line representation of the bottom and top glass panels. The heat source is connected to the Gate terminal [40]

The TFT matrix is tightly packed between two glass plates and as has no air gap or direct contact with air. Further, we have the measured temperatures at the bottom and top glass during the operation of the TFTs. This means that we have the knowledge of

the potential at node 10 and hence, we do not need to calculate the convection resistor R_convection in order to solve the heat circuit.

The heat sink is positioned at the sides of the TFT matrix in displays. The values of the interconnect resistors Rsy1, Rsy2, Rgy1, Rgy2, Rdy1, Rdy2 depends upon the length of interconnects. The TFTs are arranged in a matrix as shown in Fig 5-7 and the value of the interconnect resistors depends on the number of interconnect links from the device to the heat sink at the edges of the glass substrate.

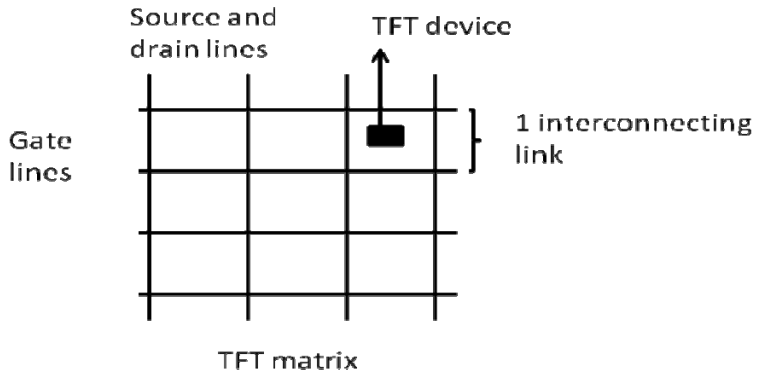

Figure 5-7: TFT matrix and one "interconnecting link" is depicted, one interconnecting link=100 µm

Table 5-2: Values of the components in the thermal circuit, along with the formulae [40]

Component	Value	Equation
Rgx	2.33kΩ	$R_k = \frac{L}{Ak}$
Rgy	83.836kΩ	$R_k = \frac{L}{Ak}$
Rsy1, Rsy2, Rdy1, Rdy2	0.2 MΩ (for one interconnecting link- refer fig 5-7)	$R_k = \frac{L}{Ak}$ (L=100 µm, that is, her is for 1 interconnecting link)
Rsx1, Rsx2, Rdx1, Rdx2	1.835 kΩ	$R_k = \frac{L}{Ak}$ (resistance of the source/drain metal pads)

Table 5-2: (Continued) Values of the components in the thermal circuit [40]

Component	Value	Equation
Rchx	$10.7 \times 10^{6}\ \Omega$	$R_k = \frac{L}{Ak}$
Rtix	$4.5 \times 10^{5}\ \Omega$	$R_k = \frac{L}{Ak}$
Cglass	2.23×10^{-9} F	100 stage transmission line was used. Only the part of capacitance directly under the device was used here. C=specific heat capacity*Mass [44]
Rglass	$5.40 \times 10^{4}\ \Omega$	$R_k = \frac{L}{Ak}$. 100 stage transmission line was used. Only the part of resistance directly under the device was used here.
Cch	1.88×10^{-10} F	C=specific heat capacity*Mass [41,42,43]
Rconvection	Not needed in simulations since we know the temperature at bottom and top glasses (equivalent to voltage at node 10)	There is no direct contact with air. The TFT matrix is packed between two glass plates
Cs	2.5×10^{-10} F	C=specific heat capacity*Mass [42,43]
Cd	2.5×10^{-10} F	C=specific heat capacity*Mass
R_lcd	$1.235 \times 10^{5}\ \Omega$	$R_k = \frac{L}{Ak}$

In LCD display panel, the heat sink is connected to the periphery of the bottom glass panel. Further, the top glass panel is in contact with air and provides cooling effect through convection. Thus, TFT devices can dissipate heat generated during operation, through the following paths: (a) interconnects which are ultimately connected to the heat sink at the edge of the glass panel, (b) the liquid crystal and the top glass panel, (c) the bottom glass panel. Among these, both the top and the bottom glass panels are bad conductors of heat, while interconnects are relatively better conductors since they are made of metals Al/Mo. Hence, the thermal behavior is dependent on the position of the device in the TFT matrix. The devices near the centre see larger interconnect resistance as compared to the devices close to the TFT matrix border which are closer to the heat sink. In order to account for this effect, we have plotted the temperature difference between the device temperature and the temperature of the glass panels for devices with different interconnect thermal resistance values.

The temperature on the top and bottom glass panels was measured during operation of the TFT display panel. The maximum temperature on the panel was found to be 45 C and the mean temperature was 40 C. For the first order simulations, we chose the temperature to be 40 C on the panel, that is, the voltage at node 10 is taken to be 40 V. The rise in temperature for TFTs with respect to the glass panels with different length of interconnect lines is shown in figs. 5-8, 5-9 and 5-10. This is temperature rise above the 40 C measured at the glass panels. Longer interconnect lengths indicate that the TFT is placed away from the TFT panel edge, which acts as the heat sink. For sake of understanding the heating effect and simplicity, we chose the Gate (G), Source (S) and Drain (D) lines to be of same lengths for each of the case. We assumed 3 cases: (a) G, S, D interconnect lines of length 100 μm each (1 interconnecting link) (fig 5-8); (b) G, S, D interconnect lines of length 1 mm each (fig 5-9); (c) G, S, D interconnect lines of length 100 mm each (fig 5-10). Thus, for a TFT with 100 mm long Gate, Source, and Drain interconnection lines (fig. 5-10), the temperature can increase up to 65 C. Simulations for all the TFTs in the LCD panel is needed for accurate understanding of the self-heating.

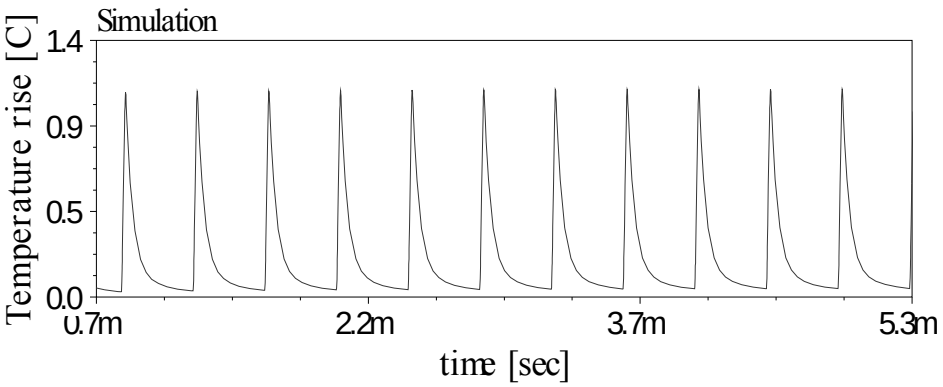

Figure 5-8: Temperature rise for all the G, S, D interconnect lines of length 100 µm each (1 interconnecting link). This temperature rise is with respect to temperature of glass panels which is 40 C

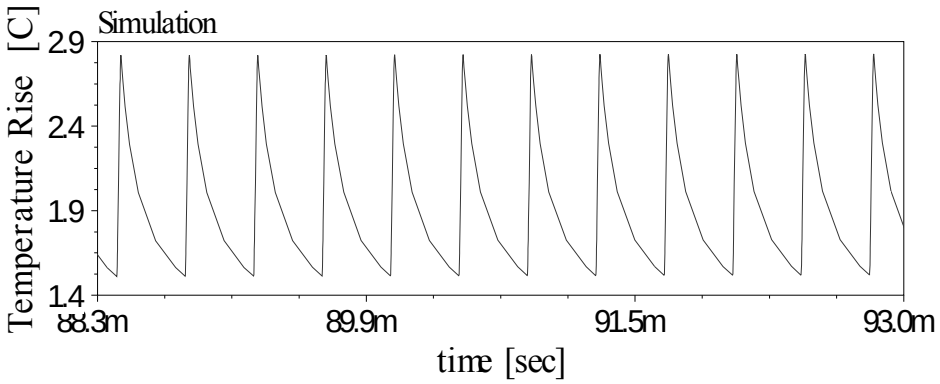

Figure 5-9: Temperature rise for all the G, S, D interconnect lines of length 1 mm each. This temperature rise is with respect to temperature of glass panels which is 40 C

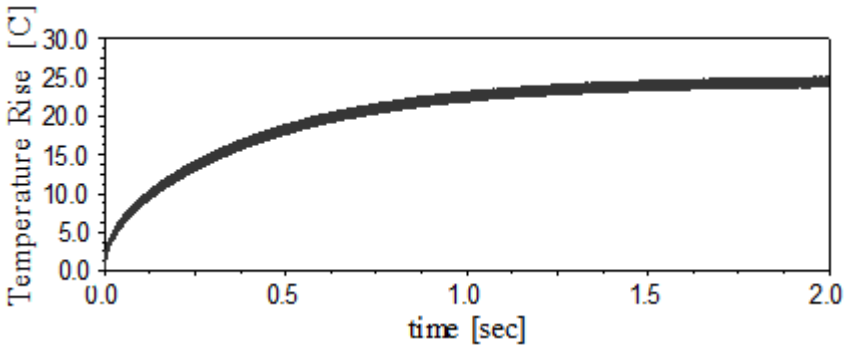

Figure 5-10: Temperature rise for all the G, S, D interconnect lines of length 100 mm each (1000 interconnecting links). This temperature rise is with respect to temperature of glass panels which is 40 C

6. Conclusion

In this work, physics-based models for amorphous Silicon thin film transistors (TFTs), including printed TFTs have been presented. The Capacitance-Voltage (C-V) characterization is described in detail and the limitations of C-V characterization are described.

A compact capacitance model for printed thin film transistors with non ideal contacts is presented. The effect of the contacts is described. The analytical description of capacitance of TFT as a function of gate bias is provided for all regimes of operation. The compact model obtained from the analytical expression for capacitance using the transmission line approach and the continuity equation was shown to have good agreement with the experimental C-V data. To account for the time constant related to the electron energy re-distribution, the Variable Dispersion Model (VDM) has been developed and implemented in AIM-Spice. The combined VDM-Elmore model is shown to reproduce the entire dispersion observed in printed TFTs. The ring oscillator simulations show that results from the combined Elmore-VDM model are significantly different from those of Elmore model, which indicates that the electron redistribution energy can have impact on the performance at even frequencies of several kHz.

The dynamic thermal equivalent circuit for a TFT pixel in LCD display has been developed and thermal simulations using AIM-Spice were shown. It was shown that for an amorphous Si TFT pixel, the temperature rise due to self heating can be noticeable. The temperature rise can be a few degrees for relatively short interconnects.

References

[1] R.L. Weisfield, M.A. Hartley, R.A. Street, R.B. Apte, "New Amorphous-Silicon Image Sensor for X-ray Diagnostic Medical Imaging Applications", Proc. SPIE Vol. 3336, p. 444-452, Medical Imaging 1998: Physics of Medical Imaging, James T. Dobbins; John M. Boone; Eds.

[2] L. Zhou; S. Jung; E. Brandon, T.N. Jackson," Flexible substrate micro-crystalline silicon and gated amorphous silicon strain sensors ", IEEE Trans. on Electron Devices, Volume 53, Issue 2, Feb. 2006 Page(s):380 – 385

[3] D. Gonçalves, D.M.F. Prazeres, V. Chu and J.P. Conde, "Detection of DNA and proteins using amorphous silicon ion-sensitive thin-film field effect transistors", Biosensors and Bioelectronics, Volume 24, Issue 4, 1 December 2008, Pages 545-551

[4] P. G. LeComber, W. E. Spear, and A. Ghaith, "Amorphous Silicon Field Effect Device and Possible Application," *Elec. Lett.*, vol. 15, pp. 179-181, 1979.

[5] DisplaySearch's Q3'07 Quarterly Worldwide Flat Panel Forecast Report.

[6] Isuppli corp. (http://www.eetimes.eu/208403538)

[7] C.-C. Tsai, K.-F. Wei, Y.-J. Lee, H-H Chen, J-L Wang, I-C. Lee, and H.-C. Cheng, "High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization", IEEE Electron Device Letters, Vol. 28, No. 11, 2007

[8] TCZ Whitepaper, http://www.tcz.com/pdf/TCZwhiteIpaper.pdf

[9] Peter V. Necliudov, " Modeling and Characterization of Pentacene Thin Film Transistors", PhD Thesis, RPI, 2001

[10] M. Shur, "Simulation, Characterization, and Circuit Design of Amorphous and Polysilicon Thin Film Transistors for Quality Control and Quality Assurance Programs in Manufacturing of High Definition Displays", RPI, 1995

[11] M.S. Shur, V. Turin and D. Veksler, T. Ytterdal, B. Iñiguez and W. Jackson, Compact Iterative Field Effect Transistor Model, Technical

Proceedings of the 2006 NSTI Nanotechnology Conference and Trade Show, Vol. 3, pg. 648 – 651

[12] H. Hao, M. Wang, B. Zhang, X. Shi, and M. Wong, "A comprehensive analytical on-current model for polycrystalline silicon thin film transistors based on effective channel mobility", J. Appl. Phys. 103, 094513 (2008)

[13] M.D. Jacunski, PhD dissertation, Univ of Virginia, 1997

[14] R. A. Street and M.J. Thompson, Appl. Phys. Lett. Vol. 45, 769 (1984)

[15] C. Taussig, M. Almanza-Workman, A. Chaiken, W. Jackson, A. Jeans, H.-J. Kim, O. Kwon, H. Luo, P. Mei, C. Perlov, F. Jeffrey, K. Beacom, S. Braymen, J. Hauschildt,"R2R fabrication of TFT backplanes using self-aligned imprint lithography (SAIL), Seminar on Flexible and R2R Electronics, MIT, 2006

[16] W. Jackson, C. Perlov, M. Amanza-Workman, S. Braymen, A. Chaiken, F. Jeffrey, J. Hauschildt, A. Jeans, O. Kwon, H. Luo, P. Mei, C. Taussig, "Electronics produced by roll to roll self aligned imprint lithography", Digest of IEEE/ LEOS Summer Topical Meeting 2007, pg. 125-126

[17] Dieter Schroder, Semiconductor material and device characterization, John Wiley and Sons Inc., 1990

[18] Agilent 4284A/4285A Precision LCR Meter Family, Technical Overview, http://cp.literature.agilent.com/litweb/pdf/5952-1431.pdf

[19] S. Blight, "The Role of CV Profiling in Semiconductor Characterization", Solid State Technology, 1990, pp. 175 – 179

[20] Y. Wang, K. P. Cheung, R. Choi, G. A. Brown, and B.-H. Lee, "Error and Correction in Capacitance–Voltage Measurement Due to the Presence of Source and Drain", IEEE Electron Device Letters, Vol. 28, No. 7, 2007, pg-640-642

[21] Y. L. Hsu, Y. K. Fang, F. C. Tsao, F. J. Kuo, and Y. Ho, "Modeling of abnormal capacitance voltage characteristics observed in MOS transistor with ultra-thin gate oxide," Solid State Electronics, vol. 46, no. 11, pp. 1941–1943, Nov. 2002.

[22] M. Shur and M. Hack, "Physics of amorphous silicon based alloy field effect transistors," J. Appl. Phys., vol. 55, no. 11 , pp. 3831-3842, May 1984.

[23] M.D. Jacunski, M.S. Shur, M. Hack, "Threshold voltage, field effect mobility, and gate-to-channel capacitance in polysilicon TFTs", IEEE Trans. on Electron Devices, Vol. 43, No. 9 , pg-1433-1440, 1996

[24] M.D. Jacunski , "Characterization and Modeling of Short Channel Polysilicon Thin Film Transistors", PhD Thesis, University of Virginia, 1997

[25] D.W. Greve, V.R. Hay, "Interpretation of capacitance-voltage characteristics of polycrystalline silicon thin-film transistors", J. Appl. Phys. 61, 1176 (1987)

[26] T. Fjeldly, T. Ytterdal, M. Shur, "Introduction to Device modeling and circuit simulation", John Wiley & Sons, 1998

[27] AIM Spice manual (www.aimspice.com)

[28] M. Shur, Physics of Semiconductor devices, Prentice Hall Series In Solid State Physical Electronics, 1990.

[29] Yuan Liu; Ruo-he Yao; Bin Li; Wan-Ling Deng, "An Analytical Model Based on Surface Potential for a-Si:H Thin-Film Transistors, Journal of Display Technology, Vol. 4, No. 2, June 2008, Page(s):180 - 187

[30] B. Iñiguez, R. Picos, D. Veksler, A. Koudymov, M. Shur, T. Ytterdal and W. Jackson, "Universal compact model for long- and short-channel Thin-Film Transistors", Solid-State Electronics, Vol. 52, No. 3, March 2008, Pages 400-405

[31] Dr. Trond Ytterdal, Norwegian University of Science and Technology, private communication

[32] M. Dyakonov and M.S. Shur, "Detection, mixing, and frequency multiplication of terahertz radiation by two-dimensional electronic fluid", IEEE Trans. on Electron Devices , 380 (1996).

[33] M. Dyakonov and M.S. Shur, "Shallow water analogy for a ballistic field effect transistor: New mechanism of plasma wave generation by dc current", Phys. Rev. Lett., 2465 (1993).

[34] D. Veksler, F. Teppe, A. P. Dmitriev, V. Yu. Kachorovskii, W. Knap, and M. S. Shur, "Detection of terahertz radiation in gated two-dimensional structures governed by dc current" , Phys. Rev. B , 125328 (2006)

[35] V. Yu. Kachorovskii and M. S. Shur, "Field Effect Transistor as ultrafast detector of modulated terahertz radiation", Solid-State Electronics, 52, pp-182 -185(2008);

[36] B. Gershgorin, V. Yu. Kachorovskii, Y. V. Lvov, and M. S. Shur, "Field effect transistor as heterodyne terahertz detector", Electron. Lett. , 1036 (2008).

[37] S. Bhalerao, A. Koudymov, M.S. Shur, T. Ytterdal, W. Jackson, C. Taussig, "Compact capacitance model for printed thin film transistors with non-ideal contacts", submitted, Intl. Journal of High Speed Electronics and Circuits.

[38] S. Bhalerao, A. Koudymov, M.S. Shur, V. Yu. Kachorovskii, W. Jackson, unpublished

[39] Ling Wang, T. A. Fjeldly, B. Iñiguez, H. C. Slade, M. Shur, "Self-heating and kink effects in a-Si:H thin film transistors", IEEE Trans. on Electron Devices, Vol. 47, No. 2, pg- 387-397, 2000

[40] S. Bhalerao, D. Veksler, S.-H. Jin, M.S. Shur, unpublished

[41] A. Mourchid, R. Vanderhagen, D. Hulin, P.M. Fauchet, "Femtosecond energy transfer in a-Si", Phys Rev B, Vol 42, No 12, 1990

[42] M. Kluge, J. Ray, A. Rahman, "Amorphous silicon formation by rapid quenching: A molecular dynamics study", Phys. Rev. B, Vol 356, No 8, Sept 1987

[43] CRC Materials Science and Engineering Handbook, p.263

[44] http://hyperphysics.phy-astr.gsu.edu/Hbase/tables/sphtt.html

[45] Dr. Dmitry Veksler, RPI, private communication

[46] F. Kreith, and M. S. Bohn, Principles of Heat Transfer, P5, PWS Publishing Co. Boston, MA (1997)

[47] K. Shimizu, S. Imai, O. Sugiura and M. Matsumura, Jpn. J. Appl. Phys. Vol. 30, No. 11A, 2664 (1991)

[48] CRC Practical handbook of Materials Science, 322 (1989)

[49] http://www.engineeringtoolbox.com/thermal-conductivity-d_429.html

[50] Dr. Alexei Koudymov, RPI, private communication

[51] Ling Wang, MS Thesis, RPI, 1998

Appendix I

The AIM-Spice circuit file for 11 stage ring oscillator is given below:

```
* Inverter sub-circuit
.subckt inv 10 20 30
* Node 10: Power Supply
* Node 20: Input
* Node 30: Output
*The device sizes taken from Samsung documents
ml 10 10 30 0 mn1 l=5u w=10u
md 30 20 0 0 mn2 l=5u w=400u
.ends inv
.model mn1 nmos level=16 asat=1 at=2e-8 blk=0.005 bt=0 dasat=0
+dd=19e-009 delta=1.01 dg=2e-007 dmu1=0.001 dvt=0.1 dvto=0.001 eb=0.78
+  eta=14 io=2e-8 ioo=1e-8 lasat=1e-8 lkink=3e-009 mkink=12 mmu=0.625 mc=3
+  mu0=1.15 mu1=0.25 mus=1.2 rd=2.75e6 rs=2.75e6 tox=27.02e-008 vfb=0.1
+ vkink=200 von=2.5
+ cgso=0.82e-9 cgdo=0.82e-9
.model mn2 nmos level=16 asat=1 at=2e-8 blk=0.005 bt=0 dasat=0
+  dd=19e-009 delta=1.01 dg=2e-007 dmu1=0.001 dvt=0.1 dvto=0.001 eb=0.78
+  eta=14 io=2e-8 ioo=1e-8 lasat=1e-8 lkink=3e-009 mkink=12 mmu=0.625 mc=3
+  mu0=1.15 mu1=0.25 mus=1.2 rd=0.6875e5 rs=0.6875e5 tox=27.02e-008 vfb=0.1
+ vkink=200 von=2.5
+ cgso=0.82e-9 cgdo=0.82e-9vdd 1 0 dc 20
xinv01 1 2 3 inv
xinv02 1 3 4 inv
xinv03 1 4 5 inv
xinv04 1 5 6 inv
xinv05 1 6 7 inv
xinv06 1 7 8 inv
xinv07 1 8 9 inv
xinv08 1 9 10 inv
xinv09 1 10 11 inv
xinv10 1 11 12 inv
xinv11 1 12 2000 inv
vnoise 2000 2 dc 0 pulse(0 0.001 1n 1n 5u 100u)
```