THE VLSI IMPLEMENTATION OF MULTIPLE INPUT MULTIPLE OUTPUT COMMUNICATION SYSTEMS

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ABSTRACT

The VLSI implementation of Multiple Input Multiple Output(MIMO) Communication Systems continue to pose a challenge to circuit designers, and stands in the way of deployment of devices to exploit the advantages of MIMO to the fullest extent. The advantages of MIMO has made it a mandatory aspect in some of the important communication protocols like the IEEE 802.16, popularly known as the WIMAX standard. In this regard, it is of utmost importance to build circuits and systems which can meet the stringent area and power requirements of present day devices.

The major bottleneck of the MIMO detection implementation lies in the detection algorithm, which, in order to gain speed and simplify the implementation to a certain extent, uses a large number of operations, all of which are not useful at the end. In this dissertation, an algorithmic modification has been proposed which can bring down the complexity of the detection algorithms by $\sim 75\%$. The proposed algorithm eliminates most of the unnecessary operations by intelligent decision feedback, and thus have a potential for lot of area and power savings.

Another drawback of MIMO detection algorithms lies in the fact that they are not only computationally complex, but also computation intensive. The algorithm is similar to a trellis decoding algorithm, where the path selections are based on path metrics. These metric computations result in very high Power $\times$ Delay product, and is a big challenge in low power design. In this work, we have simplified the metric computations to a large extent, while exploiting the regular structure of constellations used in Digital Communications. We have shown that any error resulting from the proposed simplifications can be removed at the final stage of the detector by exact operations, thus eliminating the need for exact, large word length operations, from all but the last stage of the detector. This has resulted in large power savings.

Moreover, systematic approaches to apply most of the algorithmic techniques directly on two dimensions was missing in the current literature. All reported approaches relied on intensive trigonometric computations, and were not exact. We

have proposed two different approaches to carry out efficient enumeration and path metric computations on two dimensions, which are much simplified than the reported approaches, and, though not exact, achieves the same performance as the reported approaches at a much lower cost.

Finally, an efficient resource shared architecture has been designed to implement the system in a $0.13\mu m$ CMOS technology. The proposed and implemented architecture results in heavy resource sharing, leading to a high throughput while consuming very low area and power compared to reported approaches. All results have been verified by simulations (both system level and gate level), and an FPGA implementation.