VLSI CIRCUIT AND ARCHITECTURE DESIGN OF HIGH-CAPACITY DIGITAL MEMORY SYSTEM

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ABSTRACT

Digital memory plays a more and more important role in computer system and consumer electronics. Driven by the ever exploding demand for solid-state digital memory with higher storage density, lower power consumption, and lower cost, many new memory technologies such as molecule memory, phase change memory, NAND flash memory, and magnetoresistive memory have emerged and attracted a lot of real-life interest over the past decade. This thesis concerns the circuit and architecture design for high-capacity memory systems employing these memory technologies.

Based on the molecule memory concept and the hybrid CMOS/electronic circuit, in this thesis, we designed an interconnect system serving as the peripheral circuit in the hybrid CMOS/nanoelectronic memory to interconnect between CMOS modules and nanoscale modules within memory. We present the hybrid resistor/FET-logic demultiplexer (demux) and analyze its performance in case of process variation. As a promising candidate, phase change memory possesses the advantages including short read/write time, high data-retention capacity, high sensing margin, and high scalability. Using the proposed demuxes as the address decoders, we further propose a phase change random access memory (PRAM) system with hierarchical architecture (i.e., sub-array→sub-bank→bank). We design the structure of the PRAM sub-array and the hybrid fault tolerance scheme, and investigate the impact of switching device leakage on PRAM sub-array design. Meanwhile, we propose a hybrid redundant sub-array repair and multi-bit error correction code approach to handle both random cell defects (i.e., nonfunctional memory cells) and other more catastrophic detects (e.g., broken/short rows/columns and peripheral circuit defects). NAND flash memory is the single dominant mainstream solid-state nonvolatile memory technology. Nonetheless, the aggressive scaling of NAND flash memory significantly increases the error rate. To address this storage reliability crisis, we develop a fault tolerance system for NAND flash memory based on trellis coded modulation (TCM) principle that combines the TCM system with the linear block code for error correction. We demonstrate the performance of TCM system for the NAND flash memory having the wide threshold voltage distribution versus silicon cost and latency of the hardware imple-

mentation. Furthermore, we model the cell-to-cell interference which is the main factor in NAND flash memory to distort the threshold voltage distribution, and propose an equalization approach to reduce the effects of cell-to-cell interference. Using the proposed equalization's effectiveness on decreasing the bit error rate, we present its application to increase the NAND flash memory programming throughput.