LOW-POWER CIRCUIT AND SYSTEM DESIGN IN NANOELECTRONICS REGIME

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ABSTRACT

Due to the computation intensive and hence energy hungry nature of signal processing, minimizing power consumption of signal processing systems is of great practical importance. Meanwhile, as the CMOS technology continuously scales down, increasingly severe process variability tends to make energy-efficient integrated circuits (IC) design more and more challenging. The main contributions in this thesis are the methodologies and corresponding approaches on low-power circuit and system design in nanoelectronics regime, especially for signal processing systems. [1]

In this thesis, we first present a design approach, which applies voltage overscaling to realize low-power IC implementation in the presence of process variations, and its application to trellis decoders that are widely used in data communication and storage systems. Moreover, our research also shows that realizations of the same arithmetic function using different hardware architectures may respond to voltage overscaling very differently and result in different energy saving potential. Therefore, the selection of arithmetic unit architecture turns out to be an important and non-trivial issue in voltage overscaled signal processing system design. My dissertation presents a statistical formulation for selecting the appropriate arithmetic unit architecture in voltage overscaled signal processing circuits.

Quantization in signal processing systems has a significant impact on power consumption vs. signal processing performance trade-offs. In this thesis we propose a adaptive quantization approach to implement low-power signal processing systems, which can tolerate process variations at minimal signal processing performance degradation. In this work we custom-characterize 45nm standard cell libraries to emulate process variations and demonstrate the promising energy saving potentials of the proposed adaptive quantized design solutions on FIR filter and Max-Log-MAP decoder with almost negligible performance degradation and high manufacturing yield.

Finally, as an attempt to explore innovative applications with three-dimensional (3D) memory stacking, we address application-specific accelerator design for low-power

[1] Part of work in this thesis is published or submitted to conferences or journals since 2006 [1–9].

motion estimation in video coding applications. With memory stacking technology, circuits present significant improvement on power consumption as well as performance due to much shorter interconnections and less parasitic effects. Until now, it has been rarely touched by designers to optimize signal processing systems with 3D memory stacked. Motion estimation is the most power-hungry and bandwidth bottleneck application in video codec. In this thesis we present an architecture of motion estimation and memory organization optimized for 3D stacking technology where significant power saving and performance enhancement are achieved.

All the methodologies and approaches proposed in this thesis are well demonstrated by simulations based on system-level and/or gate-level implementations of signal processing systems.