A SPLIT INSTRUCTION/DATA IMPLEMENTATION OF A STT MRAM LAST-LEVEL ON-CHIP MICROPROCESSOR CACHE

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ABSTRACT

As technological advances in microelectronics allow for the continuing downward scaling of feature size for digital logic, increasing leakage current and decreasing operating voltage become challenges to overcome in the design of microprocessors. STT MRAM is a promising new technology that offers non-volatility, low-voltage operation, and speed approaching that of SRAM and DRAM. Previous work explored the feasibility of implementing a 4MB unified L2 cache with STT MRAM on the SimpleScalar architecture. This work seeks to further explore the use of STT MRAM for this purpose by attempting to mitigate the asymmetric read/write latencies inherent to STT MRAM technology with a split instruction/data L2 cache. Simulations were done using SPICE to determine appropriate access transistor sizing. A modified version of CACTI was then used to generate caches with varying capacities and transistor sizes correlating to different write/read latencies. A modified version of SimpleScalar was used to determine appropriate capacities for the data and instruction L2 caches as well as appropriate transistor sizing for each. The resulting best-case design was then compared to a design with a 4MB unified STT MRAM L2 cache and a standard 4MB SRAM cache. Results demonstrate a decrease of 9.069% from the performance penalty associated with using a unified STT MRAM cache. Analysis of the impact of the cache design on the SPEC2000 benchmarks was also conducted.