MAGNETIC CORE INDUCTOR DESIGN AND FABRICATION FOR 3D POWER DELIVERY

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Power delivery is becoming increasingly complex as the function and integration density of integrated circuits (ICs) continue to increase. Multiple, dynamically scalable, sub-1 V supply voltages with total current exceeding 100 A/chip is required by future microprocessors. Conventional power delivery methods employing a voltage regulator module (VRM) mounted on the motherboard have some fundamental limitations in meeting future IC technology needs, such as the parasitic inductance of the interconnect, which generates large di/dt noise. This noise can cause fatal errors in computer processing.

Three-dimensional (3D) power delivery using VRM within the 3D system may be an effective solution to the problem. 3D power delivery is to stack the VRM directly on the logic circuit chip using 3D integration technology. Hence, the wire length between the VRM and logic circuits are reduced from centimeters to hundreds of microns or even tens of microns, 3 to 4 orders of magnitude improvement compared to conventional solution. The associated parasitics can be therefore greatly reduced.

Inductor is one of the key elements in VRM design, particularly its inductance (L) and inductance/resistance (L/R) ratio. For such an inductor, it is essential to use magnetic material as its core. The performance is simulated for different geometry with CoFeAlO as the selected the magnetic core material. Inductance as high as 34.1 nH and L/R ratio of 97 nH/Ω with area of about 0.03 mm^2 can be achieved with an octagon inductor with 5 layers of CoFeAlO thin film of 3 μm.

In this work, the process flow to fabricate the magnetic core inductor is designed. Each process is tested and characterized. With RF sputter method and right gas with correct ratio, high quality magnetic thin film is fabricated. The magnetic coercivity (Hc) and anisotropy field (Hk) of the magnetic thin film is 6 Oe and 50 Oe respectively, making the relative permeability to be as high as 1000. This result agrees with the simulation. Benzocyclobutene (BCB) is adopted as the inter-level dielectrics and clean etch recipe is developed with a etch rate as high as 500 nm/min. Electro-chemical Deposition (ECD) is adopted to as the method to deposit 10 μm copper and the extra copper is removed using chemical mechanical polishing (CMP). Rough and fine copper CMP recipe are developed with a polish rate as high as 0.8 μm/min. (for rough) and uniformity as good as 10% (for fine) across the wafer. Mask is designed using cadence, with inductors, transformers in different geometry and test structures for different purposes.

The design and fabrication of the magnetic core inductor paved the way to realize high efficient VRM for 3D power delivery.