

Asynchronous Parallelized Static Timing Analysis

by

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ABSTRACT

In recent year, a number of algorithms have started to make a move towards parallelization. This has been due to computers being produced with more processors rather than faster processors. However, many algorithms have trouble becoming highly parallelizable due to a large number of dependencies within the algorithm itself. Because of these dependencies, many believe that these types of algorithms cannot become massively parallel.

Static timing analysis is one of these algorithms. Static timing analysis is a useful tool for measuring the correctness of an integrated circuit. Unfortunately, there are not many methods currently available for parallelizing static timing analysis. This is due to static timing analysis being very dependent on surrounding nodes. Because of this, many of the methods for parallelized static timing analysis are not massively parallel.

Non-levelized asynchronous parallelize static timing analysis was developed in order to improve upon currently available parallelize static timing analyses. It was designed to be a massively parallel system and to compete with previously developed levelized methods. These levelized methods can prove to have a high cost of synchronization and can spend a long time waiting for other processors to finish their current level. Additionally, the levelized methods require a graph to be levelized and need to spend extra time levelizing a graph. The asynchronous method was designed to avoid these overheads.

In order to determine the relative performance increase, the asynchronous method is compared to two previously developed levelized methods which are massively parallelized static timing analyses. These comparisons are based purely on computation time and were tested to 8,192 processors on the Blue Gene/L.