Defect nucleation in Si-based devices

by

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ABSTRACT

Silicon is the most widely used material for the commercial semiconductor devices. In devices, dislocation is one of the dominant failure modes as this crystal defect leads to charge leakage and shorts.

The goal of this study is the examination of dislocation nucleation in silicon as a function of the stress state, temperature, dopant atoms, and device geometries. Large scale atomistic simulations and continuum modeling are performed to simulate the nucleation related process, e.g., nucleation of dislocation loop, transformation of dislocation core. The activation parameters are evaluated by analyzing the simulation results using reaction pathway sampling method and Arrhenius equation, and are used to characterize the dislocation nucleation quantitatively.

We have shown that the free surface corner is a favorable site for the nucleation of dislocation. The related activation energy decreases slightly with increasing the height of the ledge and has a more pronounced, non-monotonic variation with the distance between stress concentration sites. We have also shown that the Ge interstitial atoms can reduce the activation energy by changing the interatomic bonds and imposing a compressive stress on the glide plane. Furthermore, the transformation of dislocation cores from the shuffle to the glide set plane is examined. It is found that the transformation is favored by a resolved shear stress which applies no force on the original perfect shuffle dislocation. Lastly, the effect of pressure on dislocation glide plane is studied by considering the pressure-dependent γ-surface in the Peierls-Nabarro model. We show that the accuracy of the Peierls-Nabarro model can be improved by employing the generalized γ-surface instead of the regular γ-surface.