INTEGRATED CIRCUIT AND SYSTEM DESIGN FOR PERPENDICULAR MAGNETIC RECORDING READ CHANNEL

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ABSTRACT

In order to keep the historical areal density growth rate and approach the Tbit/in^2 areal density limit for the magnetic recording systems, innovative read channel signal processing and error correction coding (ECC) system design solutions are becoming increasingly indispensable. Noticeably, read channel architecture involving low-density parity-check (LDPC) code has attracted tremendous interest because of the excellent error-correcting performance and highly parallel decoding schemes of LDPC codes. Therefore there has been a great interest in replacing Reed-Solomon (RS) codes with LDPC codes in magnetic recording read channel. In this thesis, we aim to investigate key design issues in practical realization of LDPC-centric read channel from performance, silicon area and energy consumption perspectives.

First of all, we investigate the potential of applying concatenated LDPC and Bose Chaudhuri Hocquenghem (BCH) coding for magnetic recording read channel. We apply a decoding strategy that can fully utilize the bit error number oscillation behavior of inner LDPC code decoding, and its sector error rate performance down to 10^{-11} can be semi-analytically revealed. Meanwhile, based on ASIC (application-specific integrated circuit) design at 65nm CMOS technology node, we show that this concatenated coding system can have less silicon cost compared with LDPC-only and RS-only coding systems.

Since an LDPC code by itself is severely vulnerable to burst errors due to its soft-decision probability-based decoding, we further extend the above concatenated LDPC and BCH coding strategy so that it can tolerate significant burst errors in magnetic recording. A hybrid LDPC-centric concatenated coding strategy is proposed where one inner LDPC codeword is replaced by another ECC codeword with a much stronger burst error correction capability. This special inner codeword reveals the burst error location information, which can be leveraged by the inner LDPC code decoding to largely improve the overall robustness to burst errors. Using a hybrid BCH-LDPC/RS concatenated coding system as a test vehicle, we demonstrate a significant performance advantage over its RS-only and LDPC-only counterparts in the presence of three different types of burst errors.

Employing advanced iterative signal detection and coding techniques nevertheless

tends to incur large silicon area and energy consumption overhead. Motivated by recent significant improvement of high-density embedded DRAM (eDRAM) towards high manufacturability at low cost, we investigate the potential of integrating eDRAM in read channel integrated circuit (IC) to minimize the silicon area and energy consumption cost incurred by iterative signal detection and coding. We present two techniques that trade eDRAM storage capacity to reduce the energy consumption of iterative signal detection and decoding datapath. Their energy saving potentials have been demonstrated by designing a representative iterative read channel at 65nm technology node.

Finally, we propose to incorporate a lossless compressor in the read channel signal processing datapath, where it is used to reduce energy consumption in read channel IC other than saving storage space as in conventional practice. The key idea is to apply run-time lossless data compression to enable an opportunistic use of a stronger ECC with more coding redundancy in magnetic storage, and trade such opportunistic extra error correction capability to reduce average hard disk drive read channel signal processing energy consumption. Results show that up to 38% read channel energy saving can be achieved.