Architectural design Exploration of 3D- DRAMs

by

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ABSTRACT

DRAMs with their very high density and low cost form the major shareholder of the memory market and penetrate in to most of the processor based electrical systems.

With the memory and processor performance gap widening, there is a need for faster and denser memories that can bridge the gap and stand the challenges of technology scaling. 3D technology comes as a perfect solution for DRAMs in this respect. It helps them to achieve greater bandwidth, higher density and also counters interconnects related issues cropping up with scaling by reducing the global wire lengths.

In this work we look at various possibilities of designing a 3D-DRAM. Two new 3D memory designs are proposed and their power, delay and area performance are evaluated using a newly develop 3D TECH-CACTI tool. 3D vias used to connect different layers in the 3D-technolgy can cause considerable area overhead if used excessively in the design, so the proposed designs tend to minimize their use. Previously proposed 3D memory designs ignored the presence of 3D vias and tend to use them extensively unlike the designs proposed here. Comparisons in performance are also drawn between the proposed designs and standard 3D-Die packaging DRAMs that are being prototyped and produced in market.

It’s been evaluated that on an average the proposed designs yield 10-15% reduction in power (depending on the design option chosen),15-20% reduction in delay and nearly 50% reduction in the footprint with increase in every device layer in 3D when compared to an optimized 2D DRAMs.

Along with performance benefits, the proposed designs also lead to some new exciting options like increasing redundancy repair rate when compared to 2D solutions by the concept of redundancy borrow, 3D-DRAM replacing 2D SRAM as a L2 cache.