ERROR-CORRECTION CODING DESIGN AND VLSI IMPLEMENTATION FOR MULTILEVEL NAND FLASH MEMORY

By

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ABSTRACT

Driven by the ever increasing demand for on-chip/board nonvolatile data storage, Flash memory has become one of the fastest growing segments in the global semiconductor industry. Multi-level cell (MLC) storage technique, which can store more than one bit per cell, has been widely used in practice to increase Flash memory storage capacity. Owing to the inherently reduced operational margin, MLC Flash memories are increasingly relying upon on-chip error correction to ensure the storage reliability. Currently, a weak error correction code (ECC) that can only correct few errors is typically used in practice.

Higher storage capacity may be realized by further increasing the number of storage levels per cell, which nevertheless will largely degrade the raw storage reliability. Researchers have developed high accuracy programming techniques to realize 3bit/cell or even 4bits/cell storage capacity, which however complicates the design of the peripheral programming mixed signal circuits and largely degrades the programming throughput.

The main contribution of this thesis is to investigate the potential of using much stronger ECC to improve MLC Flash storage capacity. we propose to use trellis coded modulation (TCM), a widely used technique in data communication, concatenated with classical linear block codes, such as BCH (Bose-Chaudhuri-Hocquenghem) codes, to realize on-chip error correction. Based on a Gaussian-like memory cell threshold voltage distribution model and computer simulations, the effectiveness of TCM-BCH based systems, in terms of error-correcting performance and coding redundancy has been successfully demonstrated.

To investigate the trade-off between design complexities and storage capacity improvements, we designed and implemented TCM-BCH based decoders using 0.13μm CMOS standard cell and SRAM libraries. The results show that, with negligible silicon overhead, the proposed solution can enable a relatively large increase of the number of storage levels per cell and hence a potentially significant memory storage capacity improvement, while maintaining the programming throughput.