CHARACTERIZATION OF A NOVEL SELF-POWERED SOLID-STATE NEUTRON DETECTOR

By

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ABSTRACT

There is a strong interest in being able to reliably detect special nuclear materials (SNM) from illegal passage across international borders. Detectors usually use isotopes of Pu or U for detection of these materials by detecting thermal neutrons. Currently, gas-filled tube detectors are the dominant technology but they have many drawbacks. They are bulky, and require a high voltage bias for operation. There is currently much work being done investigating solid-state detectors as an effective replacement. The most basic solid-state neutron detector is a planar device where the semiconductor is covered in a conversion material. Since the semiconductor itself cannot detect the thermal neutrons, the conversion material converts them into detectable α-particles. Current conversion materials being studied include ^{10}B and ^{6}Li. These planar detectors are low-cost, simple to fabricate and easy to transport, but suffer from extremely low detection efficiencies. In order to mitigate the issues of planar detectors, deep-trenched perforated detectors were proposed and tested. These detectors boasted improved detection efficiency at the cost of more complicated fabrication and large reverse biases required for operation.

This thesis explores a further evolution of the perforated detector, a continuous p^+-n junction detector. A honeycomb-like geometry of deep trenches were filled with boron as the conversion material. This device was able to achieve neutron detection efficiencies of up to 22.5%, with theoretical efficiencies as high as 49%. There is much demand to be able to easily scale the area of these detectors. The larger the area of the device, the more easily it can detect neutrons. Scaling the device down to smaller sizes also has uses when it needs to be highly portable. This thesis examines the characteristics of the detector as the device area is scaled in sizes ranging from 1x1mm^2 up to 5x5mm^2. Both reverse leakage current density and capacitance per unit area are critical parameters involved in scaling the device, and these are looked at in depth. Relatively constant scaling for both parameters was found in addition to the leakage current density being almost 4 orders of magnitude smaller than the best result from a perforated detector.

1. Introduction

1.1 Motivation

The ability to reliably detect nuclear materials is critical to prevent the illegal transfer of these materials, which could put many at risk. Of special interest are so-called special nuclear materials (SNM), which are defined as those nuclear materials that can be used to create nuclear weapons or dirty bombs. SNM typically includes specific isotopes of plutonium and uranium. Detection of these materials may be achieved through either passive or active methods, and detecting the resultant neutron or gamma radiation. The aspect to be focused on in this paper is passive neutron detection.

In order to monitor the large amount of materials that are shipped both internationally and domestically every day, any detector created must have a high detection efficiency with a low false positive rate. It must also be easily fabricated and deployed. Ideally, the detector would also be scalable in order to allow for different detection applications. Some applications may require a larger or smaller cross-section and the efficiency of the device must not suffer greatly with these variations. It is this scaling, namely how the device parameters and characteristics scale with the device area (cross-section) that is the focus of this thesis. Several current and emerging neutron detector technologies are discussed below.

1.2 Gas-Filled Tube Detectors

The current dominant technology in neutron detection uses gas-filled tubes, which are filled with a neutron sensitive gas such as ^{3}He or ^{10}BF$_3$. An incident neutron will induce a fission reaction, resulting in an alpha particle which ionizes the gas and allows current flow.

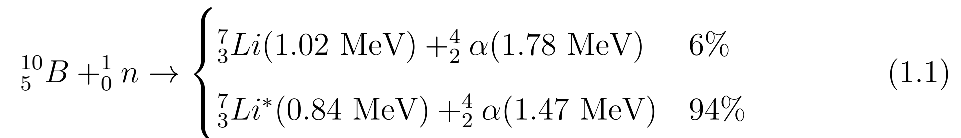
These detectors have thermal neutron detection efficiencies of about 70% [6], but are very bulky and have a high pressure internally both of which make them difficult to transport and deploy. Additionally, gas-filled detectors typically require a large bias in order to function, which can vary from about 250V to as high as

2000-3000V. All of these factors make these types of detectors less than ideal.

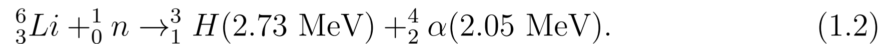
1.3 Solid-State Detectors

Another area of neutron detection is focused on solid-state detectors. These detectors are meant to generate electron-hole pairs in the presence of an incident neutron in a similar manner to photo-detectors. One major difference is that in most common semiconductor materials, most notably silicon, an incident thermal neutron will not generate an electron-hole pair and will pass by undetected. The reason for this is that neutrons are not charged particles, and thus cannot produce the electron-hole pairs necessary.

Thus, in most semiconductors a conversion layer must be used to convert the neutron into a form that an be detected, usually an alpha particle which can be detected by silicon. Common conversion layers include ^{6}Li or ^{10}B. The nuclear reactions are given by the following equations [2]:



$$ {}^{10}_{5}B + {}^{1}_{0}n \rightarrow \begin{cases} {}^{7}_{3}Li(1.02 \text{ MeV}) + {}^{4}_{2}\alpha(1.78 \text{ MeV}) & 6\% \\ {}^{7}_{3}Li^{*}(0.84 \text{ MeV}) + {}^{4}_{2}\alpha(1.47 \text{ MeV}) & 94\% \end{cases} \tag{1.1} $$



$$ {}^{6}_{3}Li + {}^{1}_{0}n \rightarrow {}^{3}_{1}H(2.73 \text{ MeV}) + {}^{4}_{2}\alpha(2.05 \text{ MeV}). \tag{1.2} $$

^{10}B has a higher absorption cross-section ($\sigma_{n,\alpha}$=3842 barns compared to $\sigma_{n,\alpha}$=955 barns for ^{6}Li) and thus a higher detection efficiency.

1.3.1 Planar Solid-State Detectors

The simplest solid-state detector using silicon is therefore a planar detector, consisting of a layer of n-type silicon below a thin p^{+} layer and then a conversion layer on top. An incident neutron will interact with the conversion layer, producing an alpha particle which will generate electron-hole pairs in the silicon p-n junction which can in turn be detected. The efficiency of this design is highly dependent on the thickness of the conversion layer. If the layer is too thick, the generated alpha particles cannot reach the p-n junction and if it is too thin then the incident neutrons will not interact with the conversion layer. In order to compute the interaction

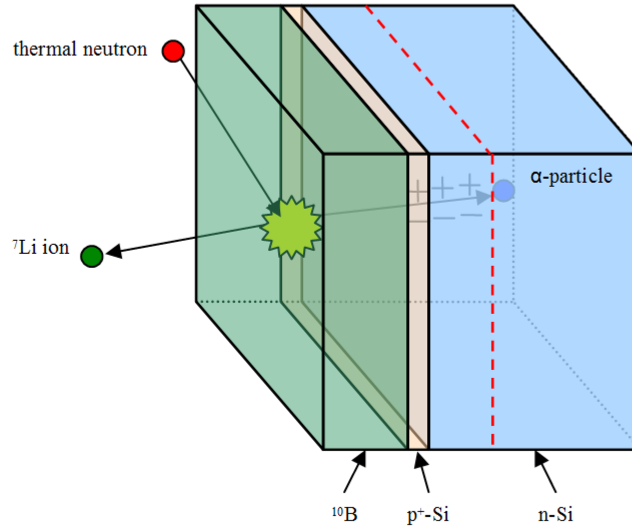


Figure 1.1: A planar solid-state neutron detector. Incident neutrons interact with the conversion layer to produce α-particles, which can be detected by the silicon *p*-*n* junction. [3]

probability of an incident neutron, the following equation can be used, where Σ_t is the total energy dependent macroscopic cross-section of the conversion material, and x_D is the thickness of the layer [7]:

$$P(x) = 1 - e^{-\Sigma_t x_D} \tag{1.3}$$

This equation is simply the inverse of the probability of no interaction. The result of this function may be seen for ^{10}B and ^{6}Li in Figure 1.2, which relates interaction probability to conversion layer thickness.

As can be seen in Figure 1.2, in order to achieve 90% interaction probability, a thickness of 45µm for ^{10}B or 550µm for ^{6}Li is necessary. Since an α-particle with an energy of 1.47MeV has a range of 3µm in ^{10}B, only about 10% of emitted α-particles would reach the silicon layer with sufficient energy (200keV) to produce a measurable result.

One proposed solution to the conversion layer problem is to make the semiconductor from a neutron-sensitive material such as boron carbide (B_4C). [9, 10] This has the effect of removing the need for the conversion layer by effectively combining

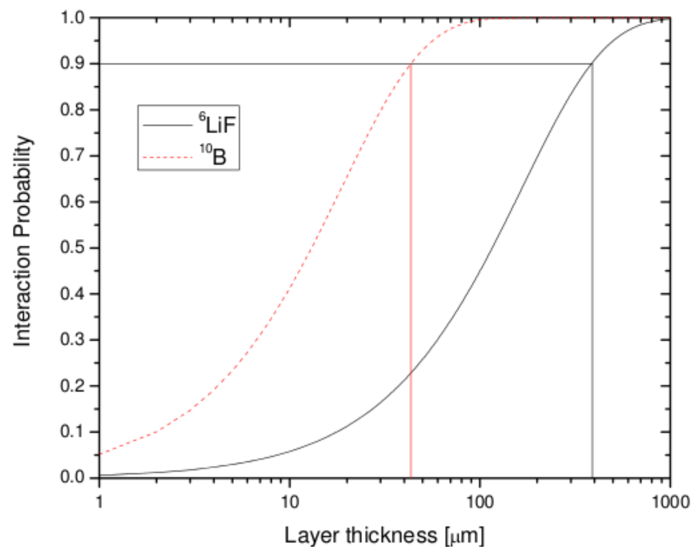


Figure 1.2: Neutron interaction probability as a function of conversion layer thickness for ^{10}B and ^{6}Li. The thicknesses required for 90% interaction probability are highlighted. [3]

it with the detector. This material also has the additional benefit of being more resistant to radiation damage due to the structure of boron carbide. The major problem with using boron carbide is that current films are of poor quality, with high defect densities. The current thickest detector able to deplete and collect charge is about 2µm thick. In order to achieve 90% interaction probability, the layer would have to be over 50µm thick for enriched boron carbide (over 260µm for natural B_4C). Current detectors using boron carbide still achieve less than 1% efficiency.

No matter the material, in order to make a planar detector with sufficient efficiency, multiple detectors must be stacked. This has some notable disadvantages, most notably giving up a low sensitivity to gamma radiation. Gamma rays typically pass through thin layers of silicon with no interactions, but can interact if the layer is sufficiently thick. Since each detector will typically be 200-500µm thick, the total stack could be as thick as 2-10mm. This thickness would be sufficient to interact with significant numbers of gamma rays and would render the detector useless in terms of selectivity. Even ignoring the selectivity issue, stacking a large number of detectors is also a fabrication challenge.

1.3.2 Perforated Solid-State Detectors

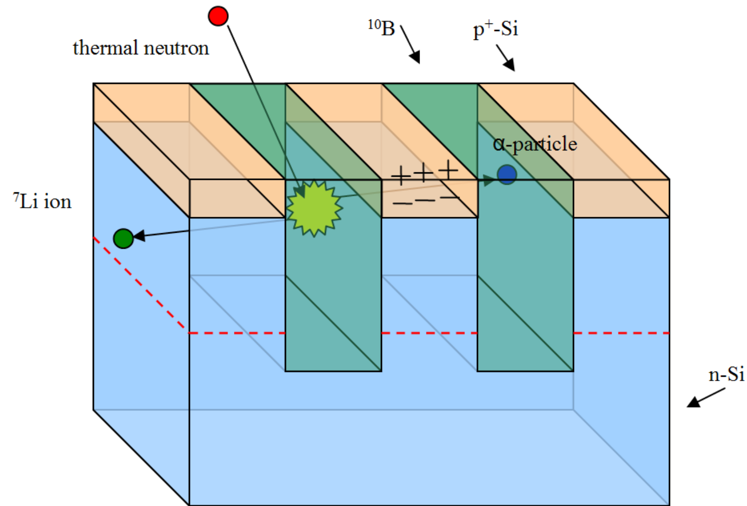


Figure 1.3: A perforated solid-state neutron detector. A reverse bias is applied to fully deplete the pillars (The edge of the depletion region is shown as a red dotted-line. [3]

One way to mitigate the conversion layer issues in the planar detector is to use what is known as a perforated detector. In this design, trenches in the bulk material are filled with the conversion layer material. The depth of the trenches is such that the incident neutrons will have enough distance to reach a very high (>90%) interaction probability. Conversely, the width of the trenches is small enough that a generated alpha particle can move to the p-n junction with a similarly high probability.

The first detectors proposed and tested using this structure used GaAs as well as Si for the semiconductor, with ^{6}Li as the conversion layer [13, 8]. This simple perforated detector, shown in Figure 1.3, has the p^{+} region along the top of the device, where the device is operated at a high enough negative voltage to sufficiently deplete the entire pillar. These perforated detectors were initially tested with very large pitch, as much as 20-100mm due to the use of ^{6}Li as a conversion material. Using ^{10}B requires smaller pitch and shallower trenches, as shown in Figure 1.2.

As mentioned, this detector design requires a large (∼15V) reverse bias in order to fully deplete the pillars. In order to avoid this requirement, an improved design

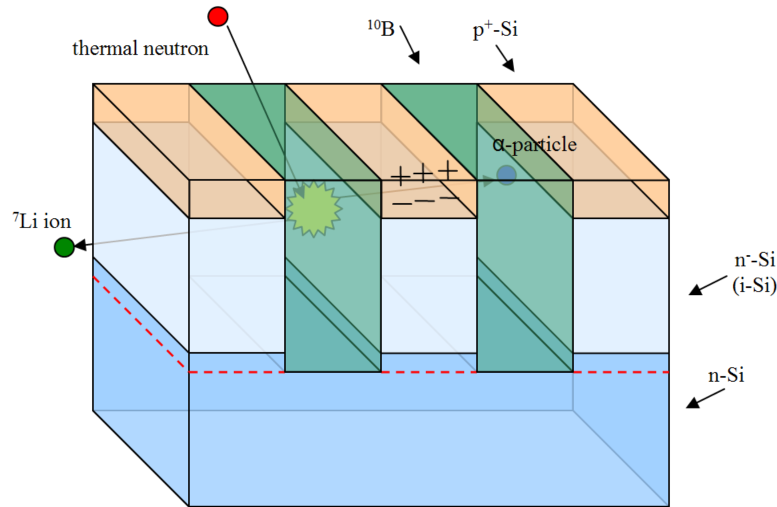


Figure 1.4: A perforated detector using a *p-i-n* diode rather than a *p-n* junction. This design requires a lower reverse bias to operate. [3]

used a *p*-*i*-*n* diode instead of a simple *p*-*n* junction [11]. A device using this design was able to achieve $7.3 \pm 0.6\%$ thermal neutron detection efficiency [12]. This design greatly reduces the necessary voltage to deplete the pillar to ∼2V. This perforated design is not without issues; it suffers from increased surface recombination as well as a large reverse leakage current. The leakage current is dominated by the surface recombination, and the lowest reported leakage current is 1.8×10^{-4} A/cm^2, which was achieved by the above-mentioned device from Nikolić et al.

1.4 Continuous P^+-N Junction Perforated Detector

An improvement to the basic perforated detector is the continuous p^+-n junction design [3]. In this design, instead of there being a *p*-*n* junction or a *p*-*i*-*n* junction at the top of each pillar, there is a continuous p^+ region along the edge of the *n*-region, creating a continuous p^+-n junction. This continuous p^+-n junction perforated detector design can be seen in Figure 1.5. It is this design that is the focus of this thesis.

Though it may seem like a small change, replacing the *p*-*i*-*n* diode with a continuous p^+-n junction has many beneficial effects. The most visible effect is to

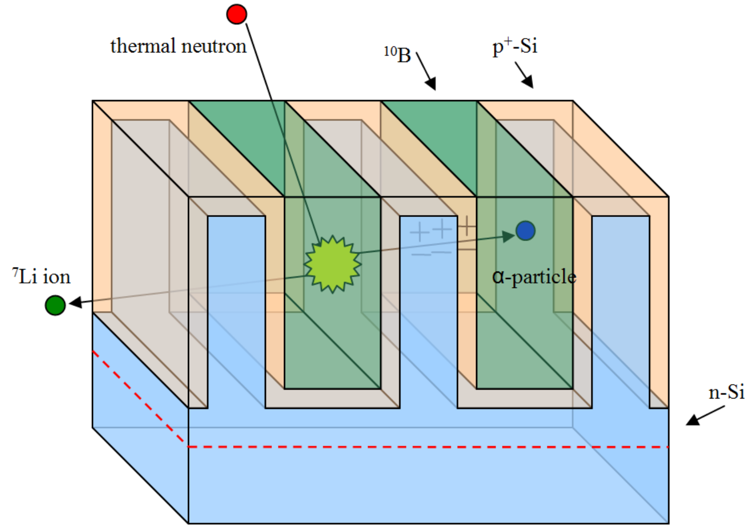


Figure 1.5: The detector design that is the focus of this thesis, the continuous p^+-n junction perforated detector. This design allows a fully depleted pillar at no reverse bias. [3]

have the pillars fully depleted under zero bias. This is achieved through careful selection of doping, such that the pillar width is less than twice the size of the depletion region. Under this condition, the depletion regions on the opposite sides of the pillar merge, allowing a fully depleted pillar. In the device used in this thesis, a background doping of $2 \times 10^{14}\,\text{cm}^{-3}$ was used (50-100 Ω-cm resistivity). There is a thin, highly doped p^+ region doped with boron to about $10^{18}\,\text{cm}^{-3}$. These choices will be discussed more in-depth in a later section.

This design also has markedly improved detection efficiency results over the planar detector as well as the perforated detectors described above. Efficiencies of up to $4.5 \pm 0.3\%$ were recorded [3]. Using enriched ^{10}B, efficiencies of up to $22.4 \pm 1.5\%$ can be achieved, the current highest published efficiency. In addition, these values are lower than predicted by simulation, which may mean that further improvements may be possible increasing the single-detector efficiency even more. Work is currently being done to investigate 3D processing of this design, which could allow the efficiency to approach very high values.

2. P-N Junction Theory

Discussion of p-n junction theory, especially I-V and C-V characteristics are treated more in depth in [1].

2.1 Formation of Depletion Region

As mentioned in Section 1.4, it is critical that the continuous p^+-n junction detector have pillars that are fully depleted. This is achieved through careful manipulation of doping and will be explored in this section. Since one of the major advantages of this design is that zero bias is necessary for correct operation, this section will be considered under thermal equilibrium so that the pillar is depleted even under no reverse bias. Additionally, the doping will be assumed to be non-degenerate.

The built in potential ψ_{bi} of a p-n junction is the difference between the Fermi levels of both sides as shown in equation 2.1,

$$q\psi_{bi} = E_g - (q\phi_n + q\phi_p) = \frac{k_B T}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right), \tag{2.1}$$

where k_B is the Boltzmann constant, q is the electric charge, T is the temperature in Kelvin, and N_A and N_D are the p-type and n-type dopants, respectively.

In order to find the depletion width from the built-in potential, the depletion approximation will be used (depleted charge has a box profile). The total charge on either side of the metallurgical junction must be equal, giving the following relationship,

$$N_A W_{Dp} = N_D W_{Dn}, \tag{2.2}$$

Where W_{Dn} and W_{Dp} are the depletion region width on the n and p sides, respectively. The Poisson equation can then be used, assuming complete ionization, to

give the electric field,

$$\mathscr{E}(x) = \begin{cases} -\frac{qN_A}{\varepsilon_s}(x + W_{Dp}) & \text{for } -W_{Dp} \leq x \leq 0, \\ -\frac{qN_D}{\varepsilon_s}(W_{Dn} - x) & \text{for } 0 \leq x \leq W_{Dn}. \end{cases} \tag{2.3}$$

The maximum electric field $|\mathscr{E}_m|$ can be found at x=0.

Manipulation of the above equations yields for the n-region,

$$W_{Dn} = \sqrt{\frac{2\varepsilon_s \psi_{bi}}{q} \frac{N_A}{N_D(N_A + N_D)}}, \tag{2.4}$$

where ε_s is the dielectric constant for the semiconductor. Similarly, for the p side,

$$W_{Dp} = \sqrt{\frac{2\varepsilon_s \psi_{bi}}{q} \frac{N_D}{N_A(N_A + N_D)}}. \tag{2.5}$$

These two equations can then be combined to give the total depletion region width,

$$W_{dep} = W_{Dp} + W_{Dn} = \sqrt{\frac{2\varepsilon_s \psi_{bi}}{q} \left(\frac{N_A + N_D}{N_A N_D} \right)}. \tag{2.6}$$

Further, since the junction in question is actually a p^+-n junction, this equation can be further simplified as seen in equation 2.7,

$$W_{dep} = \sqrt{\frac{2\varepsilon_s \psi_{bi}}{qN_D}}. \tag{2.7}$$

Once the equilibrium depletion region is known, the device capacitance can also be calculated,

$$C_{dev} = \frac{\varepsilon_s A}{W_{dep}}. \tag{2.8}$$

2.2 Current-Voltage Characteristics

The current-voltage characteristics of a *p*-*n* junction will now be considered. Starting with the ideal characteristics the quasi-Fermi levels are defined as:

$$n \equiv n_i \exp\left(\frac{E_{Fn} - E_i}{k_B T}\right), \tag{2.9}$$

$$p \equiv n_i \exp\left(\frac{E_i - E_{Fp}}{k_B T}\right), \tag{2.10}$$

where $\mathrm{E_{Fn}}$ and $\mathrm{E_{Fp}}$ are the quasi-Fermi levels for electrons and holes, respectively.

Under thermal equilibrium, the pn product is equal to $\mathrm{n_i^2}$, but under an applied voltage it is described by equation 2.11,

$$pn = n_i^2 \exp\left(\frac{E_{Fn} - E_{Fp}}{k_B T}\right). \tag{2.11}$$

pn $>$ $\mathrm{n_i^2}$ for forward bias and less than for reverse bias.

Using the continuity equations, the steady-state condition for the *n*-side can be obtained,

$$-U + \mu_n \mathscr{E} \frac{dn_n}{dx} + \mu_n n_n \frac{d\mathscr{E}}{dx} + D_n \frac{d^2 n_n}{dx^2} = 0, \tag{2.12}$$

$$-U - \mu_p \mathscr{E} \frac{dp_n}{dx} - \mu_p p_n \frac{d\mathscr{E}}{dx} + D_p \frac{d^2 p_n}{dx^2} = 0, \tag{2.13}$$

where U is the net recombination rate. Using the Einstein relation $D = (k_B T/q)\mu$ and using the low-level injection assumption the equation can be solved,

$$p_n(x) - p_{no} = p_{no}\left[\exp\left(\frac{qV}{k_B T}\right) - 1 \exp\left(-\frac{x - W_{Dn}}{L_p}\right)\right], \tag{2.14}$$

where $L_p \equiv \sqrt{D_p \tau_p}$. The hole and electron diffusions are thus:

$$J_p = -qD_p \left.\frac{dp_n}{dx}\right|_{W_{Dn}}, \tag{2.15}$$

$$J_n = -qD_n \left.\frac{dn_p}{dx}\right|_{W_{Dp}}. \tag{2.16}$$

Combining them gives the Shockley equation,

$$J = J_n + J_p = J_0 \left[\exp\left(\frac{qV}{k_B T}\right) - 1 \right], \tag{2.17}$$

where J_0 is given by,

$$J_0 = \frac{qD_p n_i^2}{L_p N_D} + \frac{qD_n n_i^2}{L_n N_A}. \tag{2.18}$$

This equation fairly accurately describes a diode in the reverse bias region at low to moderate reverse biases.

2.3 Capacitance-Voltage Characteristics

The capacitance of a p^+-n diode in the reverse bias region is dominated by the contribution of the depletion region. The equation to calculate this capacitance was given above in equation 2.8. The C-V characteristics of a p^+-n diode will be explored more in-depth in Section 3.2.

3. Continuous P^+-N Junction Neutron Detector Theory

3.1 Continuous P^+-N Junction

As mentioned in Section 1.4, the device this thesis focuses on is the deep-trenched continuous p^+-n junction detector. High aspect-ratio trenches are etched into the bulk n-type material which are then filled with the conversion layer, ^{10}B in this case. High aspect-ratio refers to the ratio between the width of the trench and its depth. The devices tested had a depth of 44µm and widths of 2.8µm and 5.0µm, for a maximum aspect ratio of 16:1. Rather than having each pillar be its own p-n or p-i-n diode where the top is p^+, the pillar is n-type with a continuous p^+-region along the surface of the trenches. The main reason for this is that such a design allows the pillars to be fully depleted even at zero bias, whereas normally in a perforated detector a negative bias anywhere from 2-15V may be necessary to achieve the same result depending on the design.

The continuous p^+-n junction does not pose a significant additional fabrication challenge either. Since the conversion material would have to be deposited in the trench on any perforated design, that poses no additional challenge. The p^+ region can then be formed by diffusion of the conversion layer boron into the bulk silicon. A more in-depth look at the fabrication process can be found in [3, 4].

As mentioned, a reverse bias is not required to fully deplete the pillars. In order to ensure that condition, the pillar widths and doping concentrations are selected for that result. In the case where the pillar is not fully depleted, there may be several causes. The pillar width may be too large for the doping concentrations used. The width should be at maximum twice the width of the depletion region, but should be at minimum large enough that the incident α-particles will interact with a sufficiently high (>90%) probability. The pillar may also fail to fully deplete in the cases where the p^+-region doping is too low or the n-region doping is too high. The major concern when changing the doping is to avoid doping the p^+-region so much that it becomes degenerate.

The dopings used are a p^+-region doping of $\sim 10^{18}\,\mathrm{cm}^{-3}$ and a bulk doping of

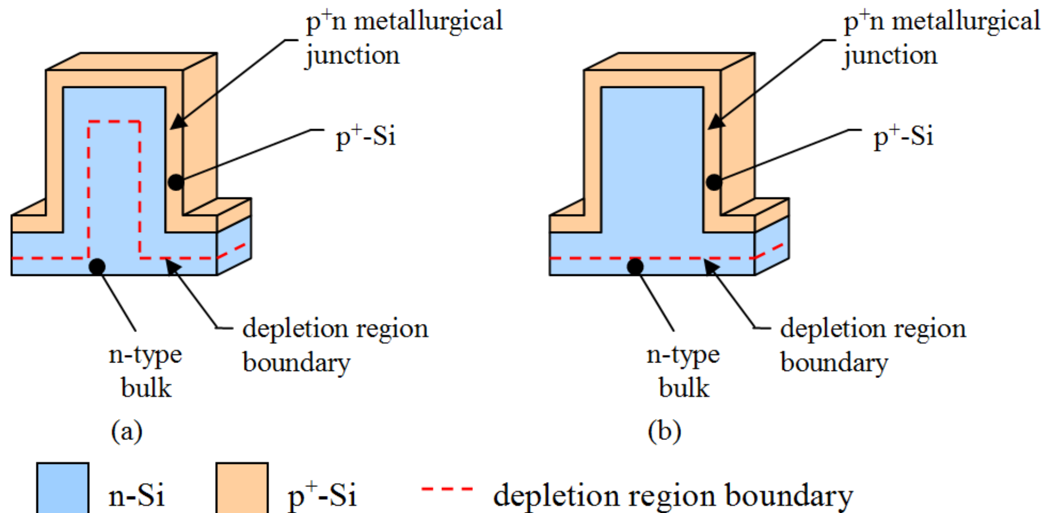


Figure 3.1: (a) A partially depleted pillar due to poorly chosen doping or pillar width. (b) A fully depleted pillar even at zero bias. [3]

$\sim 2 \text{ x } 10^{14}$ cm^{-3}. The result is that the p^+ region need only be very thin to achieve the desired result. These dopings give a maximum pillar width of 2.6µm. This was confirmed with MEDICI simulations, the result of which can be seen in Figure 3.2. In the devices used for testing, a pillar width of 1µm is used.

3.2 Device Capacitance

One sticking point of this design is that the doping and pillar width must be carefully chosen. If the doping is insufficient to fully deplete the pillar (or for some other reason), then a negative voltage will need to be applied for optimal operation, which completely negates the benefit of this technique. Further, if the pillar should not be fully depleted (such that the center of the pillar is not in the depletion region), then the device will have a much higher capacitance (∼100 times assuming 50µm pillars and 2µm spacing) due to the greatly increased depletion region surface area, as described in equation 3.1,

$$C_{dep} = \frac{\varepsilon_{Si} A}{W_{dep}}. \tag{3.1}$$

This relationship was confirmed by both hand calculations as well as simula-

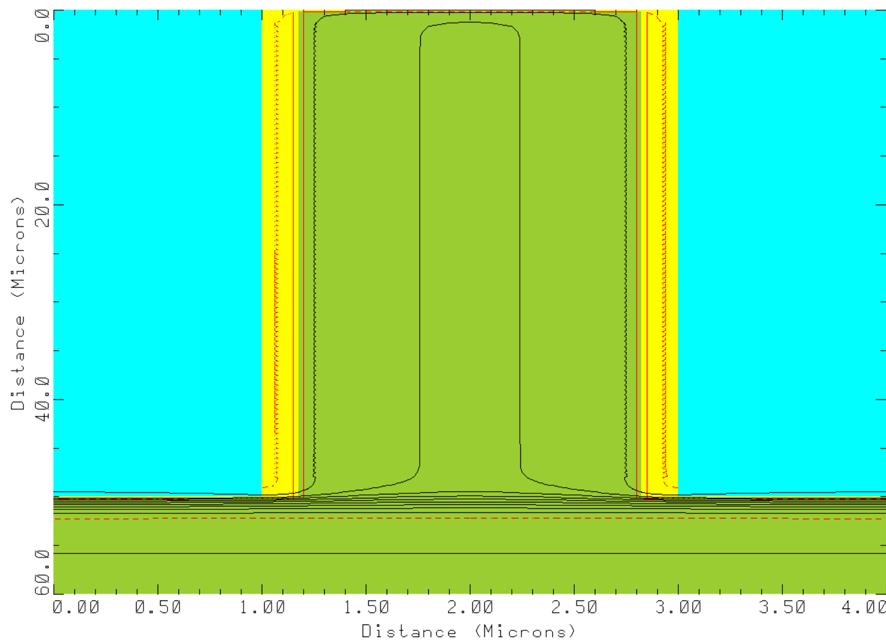


Figure 3.2: MEDICI simulations confirmed that a pillar of width 2µm will be fully depleted under zero bias. [3]

tions [3, 4]. Capacitance is critically important to the effectiveness of the neutron detector because it directly effects how easily incident neutrons may be detected. Assuming a constant injected charge Q (through conversion of neutrons to α-particles which are then converted to charge), the output voltage is inversely proportional to the device capacitance. In the case where the pillars are not fully depleted, the device capacitance is dominated by the additional surface area,

$$V = \frac{Q}{C_{dep}}. \tag{3.2}$$

Thus, reducing device capacitance is critical to improving the signal to noise ratio and ensuring accurate detection of neutrons.

A more accurate formula for capacitance may be derived, and is given here in equation 3.3 as capacitance/area [4]:

$$\frac{C_{dev}}{A_{dev}} = \frac{\varepsilon_s}{(W_{tr} + W_{pl})}\left[\frac{W_{tr}}{W_{dep}} + \frac{W_{pl} - 2W_{Dp}}{W_{dep} + h_{pl}}\right] \text{ F} \cdot \text{cm}^{-2}, \tag{3.3}$$

where W_{tr} is the trench width, W_{pl} is the pillar width, and h_{pl} is the pillar height. As a comparison, in the case where the pillar is partially depleted the capacitance will greatly increase due to a surface area that can be 100 times as large. The capacitance/area in this case is given by [4]:

$$\frac{C_{dev}}{A_{dev}} = \frac{\varepsilon_s(W_{tr} + Wpl + 2hpl)}{W_{dep}(W_{tr} + W_{pl})}\ \mathrm{F \cdot cm^{-2}}. \tag{3.4}$$

3.3 Reverse Leakage Current

In addition to determining capacitance, the geometry of the device also has a large effect on the current-voltage characteristics, especially the reverse leakage current. This current is especially important for neutron detectors due to the fact that they generally are operated in reverse bias. Generally, reverse leakage current is based on the p^+-n junction surface area, similar to the capacitance dependency. If the pillar is not fully depleted, then as mentioned there will be a much larger surface area and thus a larger reverse leakage current. In this device, the majority of the reverse leakage current is most likely due to surface effects, as the surface area of the p^+-n junction is greatly increased over a simple planar device as well as a p-n or p-i-n diode perforated device. Additionally, it was found [3] that the reverse leakage current increased after the deposition of boron. This is most likely caused by the additional stress the boron layer causes.

3.4 Device Parameter Optimization

There are several parameters that need to be optimized when designing a continuous p^+-n junction detector. The foremost concern is the size and shape of the trenches which will be filled with the conversion material. This parameter is one of the most critical to the overall efficiency of the device as well as to the ease of fabrication.

The range of a 1.47 MeV α-particle in silicon is 5.2µm [3], so feature sizes above that are unnecessary. Due to the range of neutrons in ^{10}B, a trench depth of 44µm was chosen so as to achieve 90% interaction probability. Various trench shapes were considered, the most basic of which involved long linear trenches. A more advanced

geometry saw a checkerboard pattern and the most advanced involved a honeycomb pattern. All three geometries can be seen in Figure 3.3.

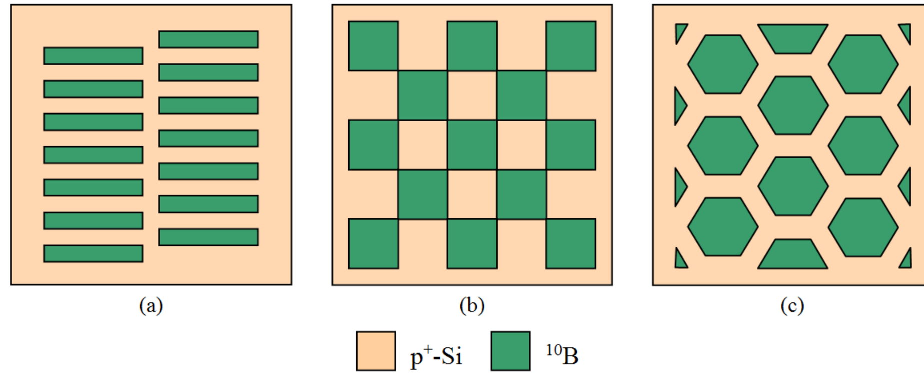


Figure 3.3: Three geometry varieties studied. (a) Linear trenches, (b) checkerboard pattern, (c) honeycomb pattern. [3]

Simulations were done on all three geometries, and the honeycomb pattern was found to be the most efficient. Further optimization was done on the pillar and trench widths to achieve a detection efficiency of 48% using trench widths of 2.8µm and pillar widths of 1µm [3], [5]. In this thesis, two sizes were tested, both of which had a 1µm pillar where one device had a 3.8µm pitch and the other had a 6.0µm pitch. Devices using these measurements were fabricated in sizes ranging from 1x1mm^2 up to 5x5mm^2.

4. Experimental Results

4.1 Device Structure

Two different devices (wafer 1 and wafer 2) were tested across a range of device areas for both current-voltage characteristics as well as capacitance-voltage characteristics. As mentioned in previous sections, the measurements used were a 44µm deep trench and a 1µm wide pillar using the hexagonal geometry. The trench widths were 2.8µm for wafer 1 and 5.0µm for wafer 2. Starting with a n-type wafer doped to $\sim 10^{14}$, the trenches were etched using DRIE and partially filled with the conversion material ^{10}B. The wafer was annealed to diffuse the boron, creating the continuous p^{+}-region. The trenches were then filled the rest of the way and contacts were placed on the top and back of the wafer. An in-depth look at the fabrication process can be found in [3]. The devices were fabricated with device areas ranging from 1x1mm^2 up to 5x5mm^2. It is the manner in which the characteristics of the device scale with the device area that is the primary concern of this thesis.

4.2 Experimental Setup

The two major parameters of concern are the current-voltage characteristics and the capacitance-voltage characteristics. In order to confirm that the devices were operational (the yield of working devices at this time can be rather low) as well as to measure the I-V characteristics over a large range, I-V measurements were taken between -5V and +1V. The top of the device was probed and a voltage applied, while the back contact was used as ground. All measurements were done within an enclosed metal box in order to minimize external photogeneration, which could skew the measured values. This is especially important when comparing the results of this thesis and published literature. A current limiter was used in order to prevent damage to the device, with a limiting value of 1mA. Voltage was swept from negative to positive in a constant linear step of 0.25V. For capacitance data, a DC voltage was swept from -5V to 0V in order to avoid damage due to there being no current limiter. An AC signal with a frequency of 1MHz was then superimposed

over the DC signal.

4.3 Current-Voltage Characteristics

Current-Voltage (I-V) characteristics are important to the operation of any device. For the continuous p^+-n junction detector, the I-V measurements help to determine if the fabricated device is working. Additionally, I-V measurements provide information on the non-idealities of the device, which can provide clues as to how the fabrication or design will affect the operation of the device. Since the device is still simply a p^+-n diode, the I-V curves reflect that. As can be expected, the I-V characteristics deviate from those of an ideal diode due to effects such as leakage current, contact resistance and series resistance. All of these effects lead to a worse signal to noise ratio and how prominent they are is important to successful neutron detection.

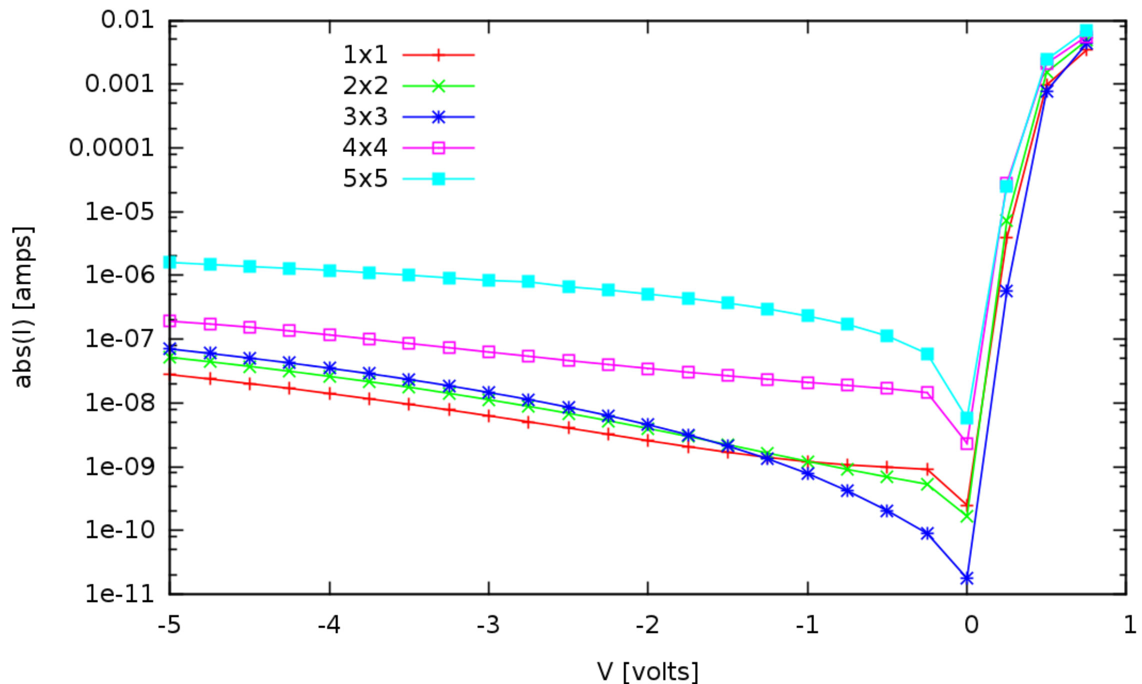


Figure 4.1: I-V characteristics for several sized devices on wafer 1.

In Figure 4.1 the whole range of square devices were tested and plotted on the same scale. There is an obvious general trend of increased reverse leakage current as

the device area increases. The 3x3 device is the one exception to the trend for low negative voltages. Considering the 4x4 and 5x5 devices exhibit expected behavior, it is safe to conclude that this is due to some other factor such as fabrication issues rather than some quirk of the device scaling. Looking at the data more closely, the important parameter is to figure out the current density(current per area), as seen in Table 4.1 for various applied voltages.

Device Area [mm^2]	Current/Area [nA/mm^2]		
	0V	-1V	-5V
1x1	0.250	-1.204	-27.900
2x2	0.042	-0.304	-13.000
3x3	0.002	-0.087	-7.833
4x4	0.146	-1.319	-11.994
5x5	0.228	-9.240	-63.840

Table 4.1: Current density in nA/mm^2 for several applied voltages and device areas.

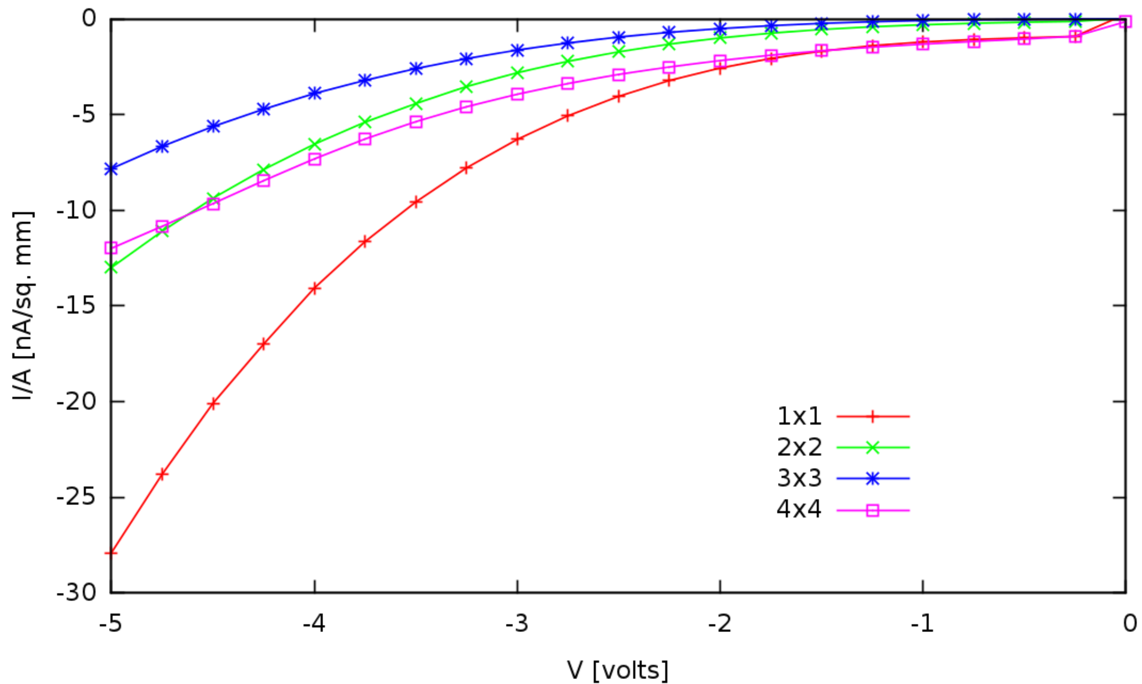


Figure 4.2: Current density in nA/mm^2 for various device sizes on wafer 1.

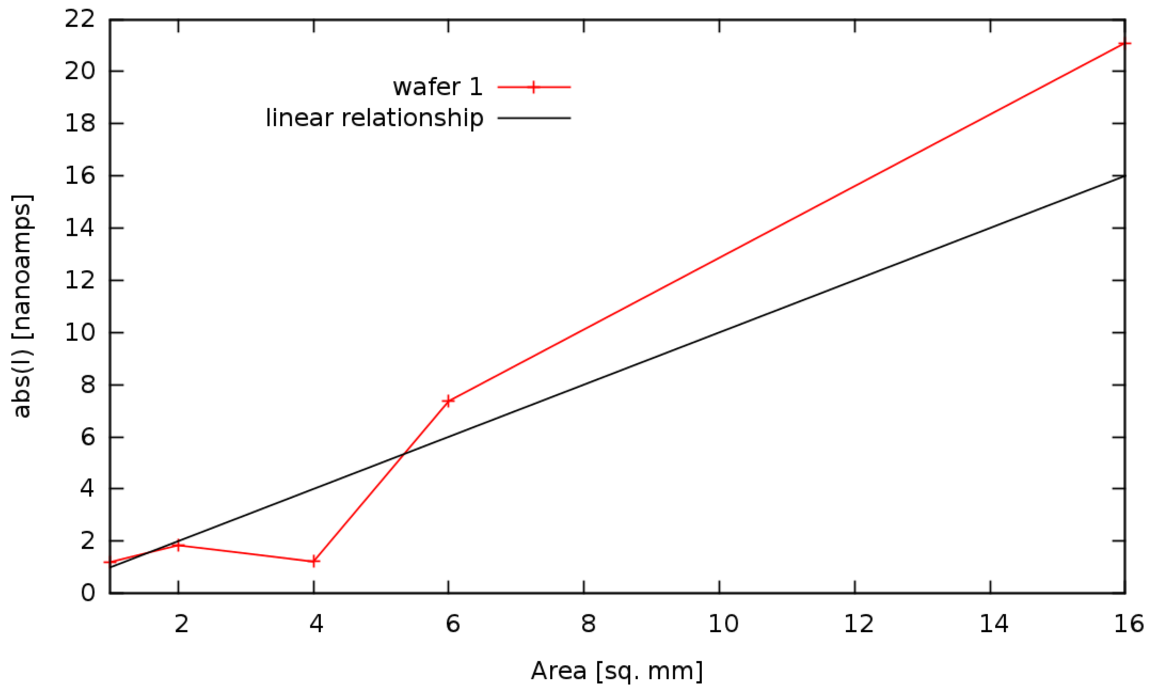


Figure 4.3: Current vs device area, showing a general upwards trend.

Generally, the absolute value of the current density increases with increasing negative voltage. There seems to be a generally expected relationship between the magnitude of the increase and the device area. At such small areas, the relationship is most likely too small and is overpowered by other factors, especially the variations in devices through fabrication and processing. The outlier in this case is the 5x5 device which has a much larger change in current density with increasing negative bias. At -1V, the value usually used for comparison, the current density values are well within an order of magnitude from each other despite the largest device being 25 times as large as the smallest, indicating that the device can be scaled up quite a lot with a negligible effect on reverse leakage current. More testing on devices in excess of 5x5mm^2 would be needed to establish if there is a relationship or not between device area and current density as well as the cause of the large deviation for the 5x5 device. A graph of these values to show the relationship is shown in Figure 4.2, with the 5x5 device size omitted for clarity.

Wafer 2 exhibits a similar relationship as wafer 1. The I-V curve for wafer 2

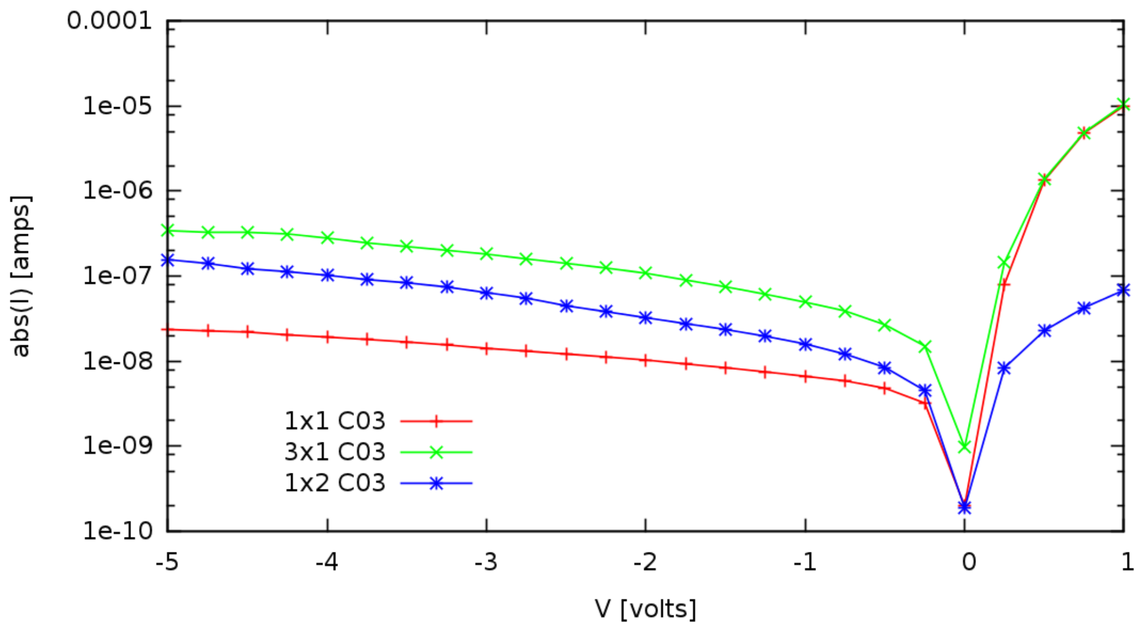


Figure 4.4: I-V characteristics for several sized devices on wafer 2.

can be seen in Figure 4.4. The devices tested on this wafer were the 1x1 square as a baseline and then the 1x2 and 3x1 rectangular wafers. Again, the leakage current increases with increasing area, but the current density remains within a small range. The change in device shape from square the rectangular did not effect the scaling, as expected.

4.4 Capacitance-Voltage Characteristics

As stated in Section 3.2, the capacitance of the detector is very important because the measured voltage is inversely proportional to the device capacitance. This relation is repeated here,

$$V = \frac{Q}{C_{dep}}. \tag{4.1}$$

If the device capacitance gets too high, the signal to noise ratio will become too poor and the detector will be unable to effectively produce output that is distinguishable from noise. Ideally, the capacitance should be minimized to make the detection of neutrons more obvious. If the pillars are not fully depleted, the ca-

pacitance will greatly increase due to its proportional relationship to the surface area. However, if the pillars are fully depleted, then the capacitance should ideally approach that of a planar detector. A planar detector in this case would be the ideal value, as there are not many things that could be done to improve the capacitance value over that.

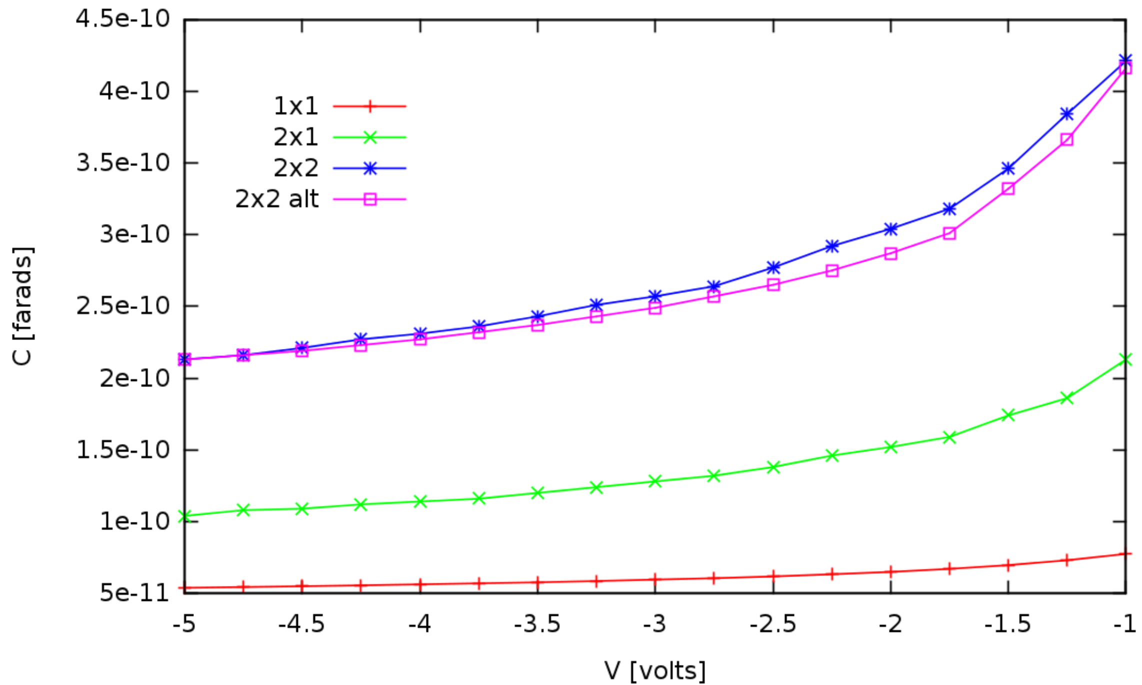


Figure 4.5: C-V characteristics for several device sizes. The 2x2 alt size is from wafer 2, the rest from wafer 1.

The capacitance measured, seen in Figure 4.5, is generally what would be expected. The capacitance increases with increasing area, because the capacitance is proportional to the area. The data that is especially of interest is the capacitance/area, seen in Figure 4.6. The capacitance/area varies anywhere from 5-10nF/cm^2, which is very close to previous simulation results [3]. Most of the data is very close together, which suggests that as predicted the capacitance is not much more than that of a planar detector. The only outlier is the 1x1 device, which deviates from the general trend more and more as the applied bias approaches 0V. The difference is small, only 3nF/cm^2 and could easily be explained as fabrication variations. The reason could also be attributable to non-ideal or parasitic effects

that only appear for low area devices. In either case, this variation is not of very much concern due to the fact that the goal is to scale the device area up, not down. Overall, the capacitance/area data is promising in terms of scaling the device to $5x5mm^2$ and beyond.

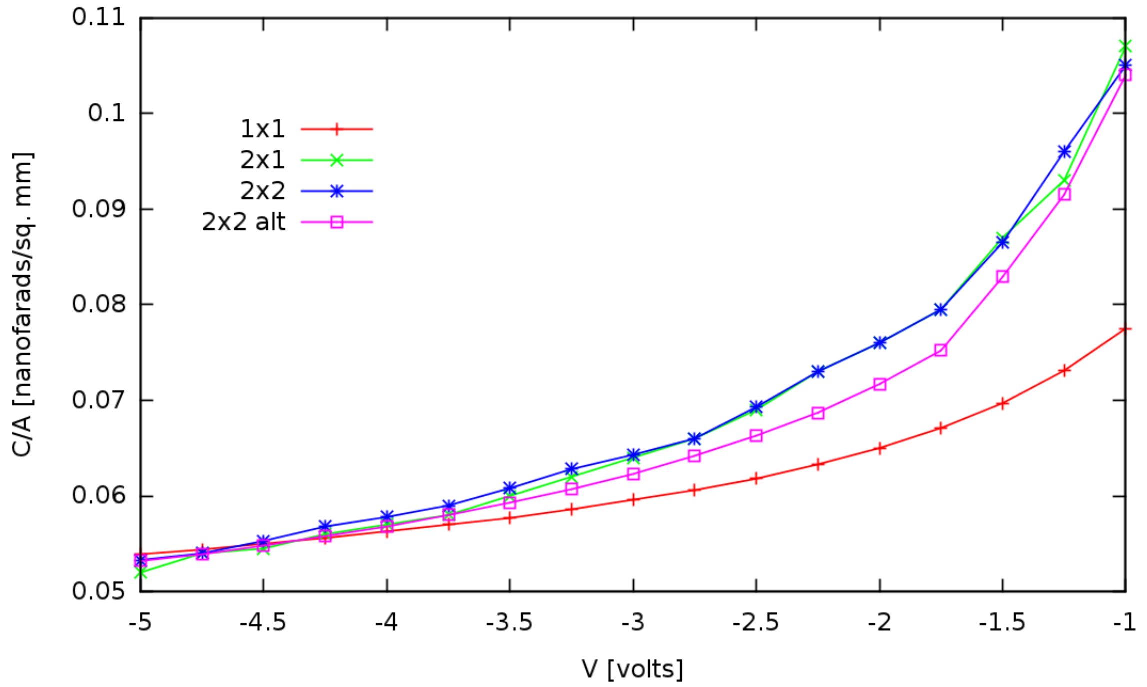


Figure 4.6: Capacitance/Area in nF/mm^2 for several device sizes.

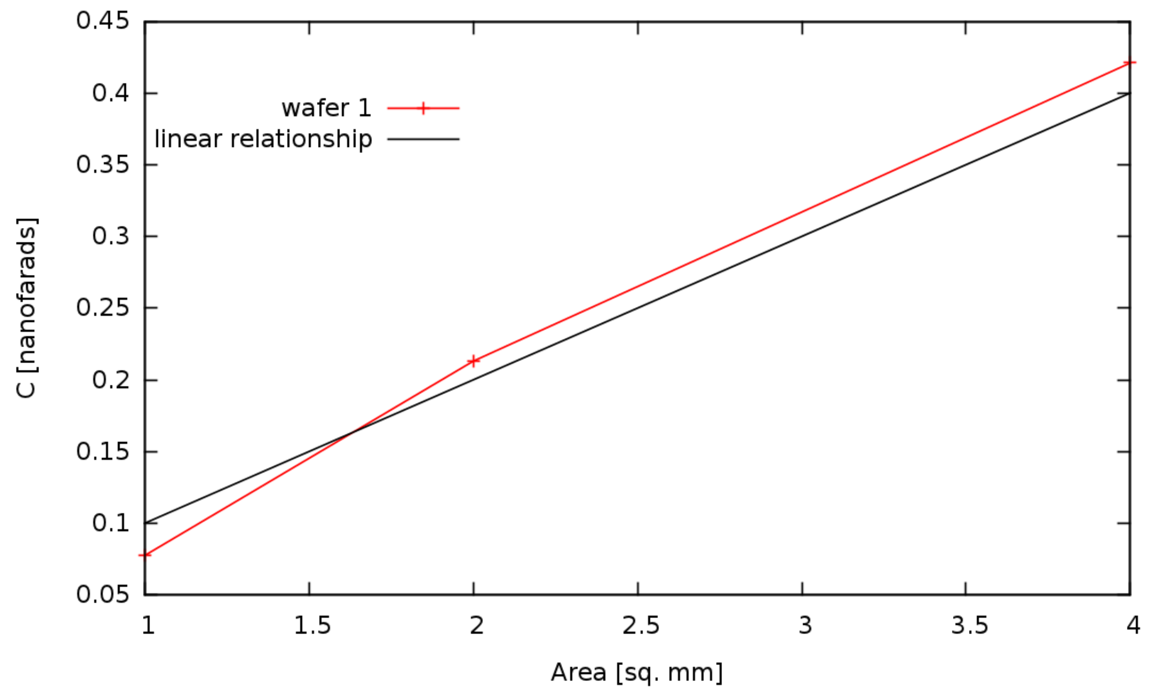


Figure 4.7: Capacitance vs device area, showing the close linear relationship.

5. Discussion of Results and Conclusions

5.1 Deviation from Theory

As discussed in Chapter 4, the experimental results do not substantially deviate from theory or simulation. The simulated depletion region in Section 3.1 showed that the pillars will be fully depleted at zero bias. This was later confirmed by both current and capacitance measurements, as those would be expected to be much higher in the case of a non-depleted pillar.

For I-V characteristics, the measured data matched up well with both simulated and theoretical data. The most visible deviation was the current density of the 5x5 device. The 1x1mm^2 device up through the 4x4mm^2 device all showed a generally linear relationship between device area and current density. Variations may be due to outside issues such as fabrication variations. Since the smaller devices showed a linear relationship between device area and current density, the result for the 5x5 device is most likely caused by fabrication variations. One other possible explanation is that the larger device area caused greater strain when depositing the conversion material, which resulted in a larger reverse leakage current than would normally be expected. More testing on larger area devices would need to be done to confirm or deny this, but unfortunately such devices had not been fabricated at the time of this writing.

For C-V characteristics, there was a similarly close match to both theory and simulation. As predicted, the fully depleted pillars allowed the device to have the depletion region area that it would have as a planar detector. This is highly ideal and a very good result for device scaling. This result was further confirmed by the tight grouping of capacitance/area data, with the exception of the 1x1 device. This exception may be caused by non-ideal effects that only become prominent at small device areas. More testing would need to be done to confirm if this was the case, especially with devices smaller than 1x1mm^2. Since smaller devices are not the focus of this thesis, further tests on 1x1 devices were not done.

5.2 Device Comparison

The two major parameters of note: reverse current density and capacitance/area were both on par or better than data in published work. The smallest reverse leakage current density for perforated detectors at the time of this writing was 1.8×10^{-4}A/cm^2 at -1V applied bias [12]. The lowest current density measured in this thesis at -1V was 8.7×10^{-9}A/cm^2 for the 3x3 device on wafer 1. However, that particular device was an outlier from the general trend. The next lowest current density was a 4x4 device at 3.04×10^{-8}A/cm^2, which is four orders of magnitude smaller than the result of Nikolić et al. Additionally, this result is smaller than the 8.8×10^{-8}A/cm^2 reported previously for a 2x2 device using this design in [3]. This reverse current density result is a large improvement over the previous work in the field, and will enable the device to scale up much larger than it would have been able to otherwise.

5.3 Device Scaling

Overall, the device scaled very well from areas ranging from 1x1mm^2 up to 5x5mm^2. The novel geometry of the device did not prevent the detector from performing well at both high and low device areas. The result of the very low (∼30nF) reverse leakage current density will enable the device to scale upwards very well. There was one troubling result for the 5x5 device, but further testing at that area and beyond would be needed to confirm whether that deviation was a result of the larger area or some other issue. Similarly, the capacitance values were very promising as well. The devices had the capacitance of a similarly sized planar device, which is close to the ideal value for this design. Additionally, the capacitance/area remained constant for larger device areas, with the only deviation being on the smallest device and thus unlikely to effect larger device areas.

5.4 Future Work

Although the results from this thesis have suggested that scaling the detector to larger sizes would not be an issue, more work still needs to be done. The most important thing would be to fabricate devices in excess of 5x5mm^2 in order to test if

the 5x5 current density result was due to the device area or due to some fabrication variation. Ideally, devices would be fabricated at much larger areas, at least up to 1x1cm^2 and possibly higher. In the opposite direction, more testing and possibly fabrication of devices smaller than 1x1mm^2 would need to be done to confirm the cause of the smaller current/area on the 1x1 device.

The next step with this detector design is to pursue 3D integration by stacking multiple detectors to reach very high detection efficiencies. In terms of device scaling, there is much work that could be done in testing to confirm that the results of this thesis remain valid in a stacked-detector environment as well as to find out how the stacking effects other device parameters. Ultimately, this detector design is intended to replace current state-of-art gas-filled tube detectors by being efficient, cost-effective, low-power and highly scalable to the specific application needed.

LITERATURE CITED

[1] S.M. Sze and K.K. Ng, *Physics of Semiconductor Devices*, 3rd Ed. Hoboken, NJ: John Wiley & Sons, 2007.

[2] G.F. Knoll, *Radiation Detection and Measurement*, 3rd Ed. Hoboken, NJ: John Wiley & Sons, 1999.

[3] N. LiCausi, "Design and Fabrication of a Novel Self-Powered Solid-State Neutron Detector," Ph.D. dissertation, Elec. Eng., RPI, Troy, NY, 2011.

[4] N. LiCausi, J. Dingley, Y. Danon, J.-Q. Lu and I.B. Bhat, "A novel solid state self powered neutron detector," *Proc. of SPIE*, vol. 7079, p. 707908, 2008.

[5] J. Dingley, N. LiCausi, Y. Danon, J.-Q. Lu and I. B. Bhat, "Optimization of a Novel Self-Powered Solid-State Neutron Detector," *Proc. Int. Conf. on Av. Math., Comp. Meth. and React. Phys.*, 2009.

[6] J.F.C.A. Veloso, F. Amaro, J.M.F. dos Santos, J.A. Mir, G.E. Deryshire, R. Stephenson, N.J. Rhodes and E.M. Schooneveld, "Application of the Microhole and Strip Plate Detector for Neutron Detection," *IEEE. T. Nucl. Sci.*, vol. 51, p. 2104, 2004.

[7] C. Petrillo, F. Sacchetti, O. Toker, N.J. Rhodes, "Solid state neutron detectors", *Nucl. Instr. and Meth. in Physics Res. A*, vol. 378, pp. 541-551, 1996.

[8] J.K. Shultis and D.S. McGregor, "Efficiencies of Coated and Perforated Semiconductor Neutron Detectors", *IEEE T. Nucl. Sci.*, vol. 53, p. 1659, 2006.

[9] A.N. Caruso, P.A. Dowben, S. Balkir, N. Schemm, K. Osberg, R.W. Fairchild, O.B. Flores, S. Balaz, A.D. Haken, B.W. Robertson and J.I. Brand, "The all boron carbide diode neutron detector: Comparison with theory," *Mat. Sci. Eng. B-Solid*, vol. 135, p. 129, 2006.

[10] R.J. Nikolić, C.L. Cheung, C.E. Reinhardt and T.F. Wang, "Roadmap for high efficiency solid-state neutron detectors," *Proc. of SPIE*, vol 6013, p. 601305, 2005.

[11] R.J. Nikolić, A.M Conway, C.E. Reinhardt, R.T. Graff, T.F. Wang, N. Deo and C.L. Cheung, "Fabrication of Pillar-Structured Thermal Neutron Detectors," *IEEE 2007 Nucl. Sci. Symp. Conf. Rec.* vol. 2, p. 1577, 2007.

[12] R.J. Nikolić, A.M Conway, C.E. Reinhardt, R.T. Graff, T.F. Wang, N. Deo and C.L. Cheung, "6:1 aspect ratio silicon pillar based thermal neutron detector filled with ^{10}B," *Appl. Phys. Lett.* vol. 93, p. 133052, 2008.

[13] D.S. McGregor, R.T. Khan, H.K. Gersh and J.D. Sanders, "Designs for Thin-Film-Coated Semiconductor Thermal Neutron Detectors," *IEEE 2001 Nucl. Sci. Symp.*, vol. 4, p. 2454, 2001.