Coding of a Novel Stochastic Impulse-Response Extraction Algorithm for *RC* IC-Interconnect Networks

by

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A Thesis Submitted to the Graduate

Faculty of Rensselaer Polytechnic Institute

in Partial Fulfillment of the

Requirements for the degree of

MASTER OF SCIENCE

Major Subject: Computer and Systems Engineering

Approved:

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August, 2007

ABSTRACT

The interconnect characteristics of high-end digital ICs will have an increasing influence on performance as device density and operating frequency rise. Modeling IC-interconnect performance requires both an accurate calculation of physical phenomenon and an appropriate discretization of the equivalent-circuit network. Existing software computer-aided-design (CAD) tools are not suitable for analyzing increasingly dense, massively-coupled networks (more than 1G interconnect wires). Additionally, these tools are not designed for possible future interconnect technologies, such as carbon nanotubes (CNT) or ballistic nanowires. Utilizing a novel *RC* IC-interconnect impulse-response extraction algorithm, a prototype software kernel has been developed in C to calculate first- and second-order impulse-response moments for arbitrary *RC* IC networks. These networks were evaluated stochastically by means of Monte Carlo sampling.

For the first-order moment (m_1) a two-wire test circuit consisting of three, five, and ten resistor-capacitor "stages" was analyzed. The impulse-response moments generated by our coded algorithm were within 10% of the analytically exact values after only 1K samples, and within 0.5% after 1M samples. These calculations were performed on a 2-GHz *Pentium M*™ processor which, for reference, completed the 1M-sample execution in less than two seconds.

A similar test was conducted for the second-order moment (m_2) program, using a three-wire test circuit with one, three, and five stages. The impulse-response moments calculated by our program were within 23% of the exact values after only 1K samples, and within 1% after 1M samples. (These are worst-case results. Most calculations were within 10% after 1K samples, and 0.5% after 1M samples.)

Future extensions of this prototype kernel would involve generation of third-order and higher impulse-response moments. Additionally, a *RLCM* interconnect model could be developed to provide an even better representation of high-frequency IC-interconnect behavior.