Changes in electrical and thermal parameters of LED packages under different current and heating stresses

by

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Abstract

The goal of this dissertation is to identify electrical and thermal parameters of an LED package that can be used to predict catastrophic failure real-time in an application. Through an experimental study the series electrical resistance and thermal resistance were identified as good indicators of contact failure of LED packages. This study investigated the long-term changes in series electrical resistance and thermal resistance of LED packages at three different current and junction temperature stress conditions.

Experiment results showed that the series electrical resistance went through four phases of change; including periods of latency, rapid increase, saturation, and finally a sharp decline just before failure. Formation of voids in the contact metallization was identified as the underlying mechanism for series resistance increase. The rate of series resistance change was linked to void growth using the theory of electromigration. The rate of increase of series resistance is dependent on temperature and current density. The results indicate that void growth occurred in the cap (Au) layer, was constrained by the contact metal (Ni) layer, preventing open circuit failure of contact metal layer. Short circuit failure occurred due to electromigration induced metal diffusion along dislocations in GaN. The increase in ideality factor, and reverse leakage current with time provided further evidence to presence of metal in the semiconductor. An empirical model was derived for estimation of LED package failure time due to metal diffusion. The model is based on the experimental results and theories of electromigration and diffusion.

Furthermore, the experimental results showed that the thermal resistance of LED packages increased with aging time. A relationship between thermal resistance change rate, with case temperature and temperature gradient within the LED package was developed. The results showed that dislocation creep is responsible for creep induced plastic deformation in the die-attach solder. The temperatures inside the LED package reached the melting point of die-attach solder due to delamination just before catastrophic open circuit failure.

A combined model that could estimate life of LED packages based on catastrophic failure of thermal and electrical contacts is presented for the first time. This model can be used to make a-priori or real-time estimation of LED package life based on catastrophic failure. Finally, to illustrate the usefulness of the findings from this thesis, two different implementations of real-time life prediction using prognostics and health monitoring techniques are discussed.

1 Background

Light emitting diode (LED) technology is gaining acceptance as the light source for a variety of applications [1]. Energy savings, color tunability, ease of developing controls and long life times are some of the claimed advantages of this technology [2], [3]. Many innovations have immerged in the LED lighting space, utilizing many unique features of LEDs to enhance delivered value to users. Presently, the LED lighting industry defines the life as the time taken for the light level to depreciate to 70% of the initial value [4]. However, in practical applications there is no means to know when a light source has reached end of life based on this definition. Furthermore, in applications a system can reach end-of-life by ceasing to produce any light, known as catastrophic failure. Such failures are problematic in certain critical applications. In aviation, aerospace, automotive, street lighting, signaling and industrial applications, unscheduled failures of lighting systems compromise safety and increase operational costs [5], [6], [7], [8]. Therefore, an early warning methodology could improve safety, and reduce operational costs.

Such a feature built into a fixture enhances the delivered value to users of lighting systems where cost of failure and cost of maintenance is critical. The main questions is, what key parameters in an LED package can be measured in real time that could provide reliable indication that the LED package is about to fail. Therefore, the goal of this dissertation is to identify electrical and thermal parameters of an LED package that can be used for predicting failure ahead of failure while in use.

An LED lighting system is composed of many different sub-systems, such as LED packages, a thermal management system, secondary optics, and an electrical driver unit. Failure of one of these sub-systems would affect the performance of an LED lighting system. Each of these sub-systems consists of many different components. This dissertation focuses on catastrophic failure prediction of an LED package when subjected to temperature and current stress conditions.

Degradation of contacts in the LED package could lead to catastrophic failure and the probability of contact failures is significant in the reliability assessments. Further, immerging trends in LED packaging industry such as, high density packaging, high temperature rated LED packages, and high current density packages have made reliability of electrical and thermal contacts a significant concern.

Electrical and thermal parameters indicate the health of the package's electrical and thermal conduction paths. Therefore, measuring and analyzing the changes of these parameters could act as early predictors of catastrophic failure. Further, these parameters can be measured real-time within the application environment, reliably at reasonable accuracies. The systematic study of these parameters during early and late stages

specifically close to the end of life can indicate the dominant failure mechanisms of electrical and thermal contacts. This is invaluable for improving LED package design for reliable operation. The following sections of this chapter will provide an introduction to components in an LED package, LED package types, and reliability practices in the LED packaging industry.

1.1 Definition of key terms

Key terms that have been used in thesis are defined below.

LED die: “A small block of light-emitting semiconducting material on which a functional LED circuit is fabricated [9].”

LED package: “An assembly of one or more LED dies that include wire bond or other type of electrical connections, possibly with an optical element and thermal, mechanical, and electrical interfaces. Power source and ANSI standardized base are not incorporated into the device. The device cannot be connected directly to the branch circuit [9].”

LED array: “An LED array is defined as two or more individual LED chips mounted in a package or on a substrate in a manner such that any device in the array can be powered through either series, parallel or individual connections while the other devices in the array may or may not be operating. The individual LED chips may also consist of an array of LED junctions on the chip as well [10].”

LED luminaire: “A complete lighting unit consisting of LED-based light emitting elements and a matched driver together with parts to distribute light, to position and protect the light emitting elements, and to connect the unit to a branch circuit. The LED based light emitting elements may take the form of LED packages (components), LED arrays (modules), LED Light Engine, or LED lamps. The LED luminaire is intended to connect directly to a branch circuit [9]”.

Parametric failure: The product functions but operates outside its specifications. In the case of general illumination, parametric failure is defined as the point at which light output depreciate below 70% of its initial value [4].

Catastrophic failure: Complete failure of the product. In the case of LED package this would mean no light emission from the device.

1.2 LED Package

An LED package is comprised of many different components, such as LED die, contact metallization layer, wire-bonds, solder layer, a sub-mount, a substrate die-attach layer, an encapsulant, a phosphor layer, and a lens. An illustration of an LED package is given in Figure 1. All these elements are different material systems. There is a considerable overlap in the different types of LED packaging materials used in the industry. However, there are different packaging methodologies, chip-on-carrier-substrate, flip-chip, chip-on-insulating-substrate, multi-junction, and multi-die array, that may be unique to a particular manufacturer. These designs would have pros and cons in terms of their cost, size, and reliability.

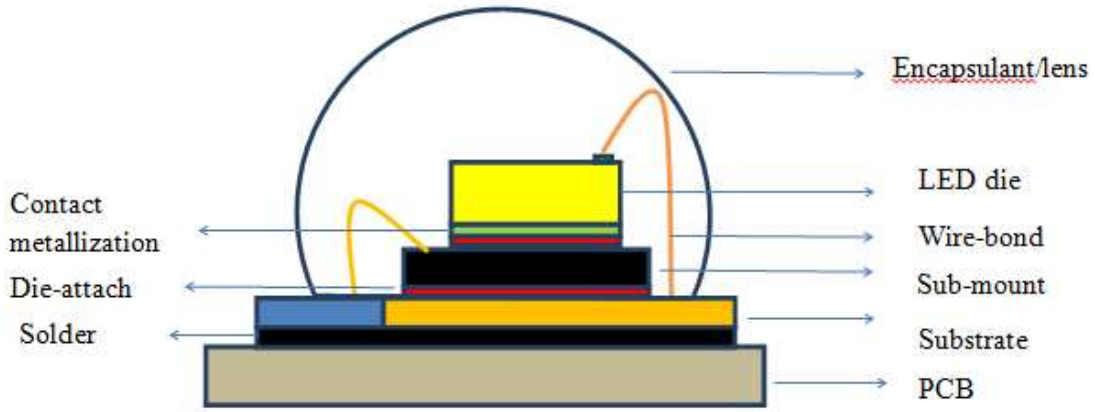


Figure 1. Cross-section of an LED package

1.2.1 LED die

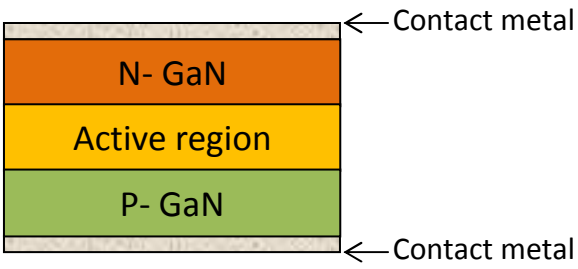


Figure 2. Cross-section of a vertical GaN based LED die

The architecture of an LED die will consist of multi-quantum well active region, electron/hole blocking regions, buffer layers, growth substrates, ohmic contact

metallization layer, and passivation layer. The InGaN multi-quantum well active region is the emission layer of the die in GaN-based LEDs. This is the P-N junction region where the electron-hole recombination takes place. This recombination of electrons and holes could be radiative or non-radiative. The radiative recombination would lead to emission of radiant energy, with a peak emission wavelength determined by the band-gap of the material. The non-radiative recombination will generate heat which needs to be conducted from the semiconductor to the ambient. There are different material systems (ex: GaAs, GaP, GaN) that have been studied for their light emission properties.

The focus of the thesis is LED packages that use GaN material system. The first reported synthesis of GaN happened in 1932 through chemical reaction of Ga and NH_4 at elevated temperatures of 800^0C-1000^0C [11]. Even though its high band-gap offered benefits in optoelectronic applications, device fabrication issues hindered the widespread use of this material [12]. The innovations in the GaN growth process by Nakamura et al. at Nichia Corporation enabled the current developments in GaN in optoelectronic applications [13], [14], [15], [16].

1.2.2 Ohmic contact

All electronic devices require an electrical connection to function in their applications. In the case of LEDs these connections need to be provided to both p-type and n-type regions of the semiconductor. Ideally these electrical connections should not interfere with the performance of the device. The voltage drop across these contacts should be proportional to current so that the device is not subjected to unpredictable non-linear effects. In other words the electrical connections should follow Ohms' law and therefore, is referred to as ohmic contacts. High quality ohmic metal contact in the context of high power LEDs should have the following properties.

- It should have low specific contact resistance.
- It should have high transmittance or reflectance within the emission wavelengths of interest, depending on the package type.
- It should form thermally stable material phases with the semiconductor at the contact interface.

All of the above attributes play a critical role in device performance in the short and long-term. The high contact resistance leads to joule heating at the vicinity of the semiconductor which would have a negative effect on device efficiency and reliability. The poor optical properties lead to lower light extraction and therefore, poor device efficiency. The undesirable optical characteristics of ohmic contacts would mean that device designers have to reduce the coverage area of the metal contact in the die. This leads to high current densities in thin metallization layers that cause long-term reliability

issues. The formation of thermally stable phases between the metal and semiconductor is important to prevent diffusion of metal atoms into the semiconductor, and for long-term adhesion of the two materials.

Even though it's desirable to have all of the above mentioned properties in the electrical contact, in reality device designers have to compromise between different attributes. The formation of low resistance ohmic contact to GaN-based LEDs is itself a challenge to the limited choice of compatible metals and alloy compositions. The fundamental physics of metal-semiconductor contacts provides an insight into this challenge. The basic physics of metal-semiconductor contacts and recent developments in ohmic contact formation in GaN is explained in appendix A.

1.2.3 Die-attach material

The die-attach layer provides a mechanical attachment between two material layers. The quality of the attachment determines the conduction heat transfer within the package. The junction temperature of the LED determines its light output, color, and reliability. The packaging materials and design determine the junction temperature of the LED package. Die-attach materials have low thermal conductivity when compared to other material layers; thus, act as a critical bottleneck in the heat conduction path.

There are two main types of die-attach materials, organic adhesives with metal particles, and solder alloys [17], [18]. In the organic adhesives, metal particles are suspended in a polymer binder such as epoxy, silicone, or a polyimide. The curing temperatures of the adhesives are around 150^0C-200^0C, whereas lead free solders have melting points greater than 250^0C. The solder alloys have low thermal and electrical conductivities. They also have low resistance to thermal fatigue when compared to metals [18]. The use of solder pastes with large dies leads to formation of voids that worsen the thermal transport properties and increase stress conditions. As a solution to these problems, semiconductor industry has investigated the use of Ag and its alloys as die-attach materials. The eutectic $Au_{80}Sn_{20}$ die-attachment process is widely used in LED packages, due to better thermal properties and high mechanical strength when compared to the choices discussed above.

The key factors that determine the quality of the eutectic die attach is the structure of the die metallization layer, the substrate pad metallization layer, and the bonding temperature profile [19]. Evaporation and electroplating techniques are used by the industry to form a well-controlled (composition) metallization layer at the back side of the die. The Ni/Au bond pad at the substrate is used to provide a good wetting surface. When exposed to high bonding temperatures Au will migrate into $Au_{80}Sn_{20}$ layer and form an Au rich metallization layer. However, if the exposure time is prolonged then Ni will diffuse and form Au-Ni-Sn, inter-metallic compound which has a lower mechanical strength.

Therefore, thickness of the Au layer at the bond pad should be optimized to prevent Ni migration [19], [20].

1.2.4 Wire-bond

Wire-bonds are used in LED packages mainly for electrical contact purposes. The wire-bonding technology is a mature technology that is widely used in integrated circuit(IC) packaging industry. The wire-bonding is a solid state welding process where a contact between two metals is formed through diffusion. The force required to facilitate this diffusion process is provided through temperature, vibration, and force. Based on the combination of factors used to facilitate diffusion, wire-bonding technologies can be divided in to three groups, thermo-compression (temperature and force), thermo-sonic (temperature, vibration and force), and ultrasonic (vibration and force). Thermo-sonic bonding technology is widely used for Au wire-bonding to Au/Al bonding pads. Since these are the most common types of materials used in LED packages, thermo-sonic bonding is widely used in LED industry.

There are two types of wire-bonds: wedge-ball bonds and wedge-wedge bonds. Typically at the semiconductor die, wire-bond is a wedge bond whereas at the substrate it's a ball bond. The wedge bond has the advantage of deep access and finer pitch. However, the bond formation is a slower process when compared to ball bonds. Au is the material of choice for ball bonding because other candidate metals such as Al and Cu oxidizes rapidly during the bond formation process. Au wire on Au metallization pad can form reliable bonds since probability for corrosion and intermetallic formations are limited. Overall bond quality depends on the design of the wedge, mechanical properties of the wire, quality and thickness of the substrate metallization, capabilities of the wire bonder, and optimization of bonding force, temperature, and bonding time [21]. There are three failure modes in the bond formation process; no bond formation, complete lift-off of the bond during testing, and heel break leaving a portion of the wire bond at the die pad during testing.

1.2.5 Substrate

The substrate of an LED package also plays a critical role in terms of heat conduction and mechanical stress management. In some LED packages the die is attached to a submount (Si or SiC) using a thin solder/epoxy layer and then the submount is attached to the substrate. The chip-on-board technology is where the die is directly attached to the substrate. The thermal conductivity, the thermal expansion coefficient mismatch with the die or submount, and elastic modulus are key considerations in determining material

choices for LED packages. In terms of thermal conductivity popular substrate choices could be ranked from worst to best as, FR4 (glass fiber reinforced in epoxy), ceramic - Al_2O_3, ceramic- AlN, and metals [22].

Ceramic substrates have a lower CTE mismatch with Si-based submounts when compared with metals. This leads to lower stresses at the interface. However, the Young's modulus mismatch between ceramic and submount is significant. Therefore, if the package is subjected to cyclical stresses there is a possibility for crack formation in the ceramic substrate. Metals have the highest thermal conductivity of all substrate choices but also have high thermal expansion coefficient mismatch.

1.2.6 Encapsulant

The encapsulant is an important element of the LED package that acts as, a hosting medium for phosphor, a facilitator for photon extraction, and a capping lens. Material properties such as, thermal stability, refractive index, optical transmission, photo-chemical stability, and viscosity are key considerations for LED package development. The refractive index determines the external quantum efficiency of the LED. Higher refractive indexes in the range of 1.8-2.5 are desirable for light extraction purposes [23].

The direct emission wavelengths of nitride LED dies range from near UV to 470nm. It is important that the encapsulant material is stable at this wavelength regime and has high optical transmission. The heat generated at the junction and down conversion losses in the phosphor heat up the encapsulation layer. Therefore, thermal stability at high temperatures is an important consideration when selecting materials for encapsulation. Few years back, epoxy was the most commonly used encapsulation material. The emergence of thermally stable silicone has replaced epoxy as the encapsulant in high power LED packages.

1.3 LED package types

LED packages available in the market could be classified into various categories. They could be classified in terms of the number of dies in a package, single die vs. multi-die arrays. In a multi-die array LED package multiple dies attached directly to a substrate (metal or ceramic) is connected using wire-bonds in series parallel configuration. The advantage of this package is its high flux density. The multi-junction LED package consists of multiple junctions formed vertically and laterally using a network of blocking diodes and electrodes [24]. ITO is the commonly used electrode due to its high optical transmittance. However, these devices have high series resistance. These packages can be

operated at high voltages, therefore has significant benefits in power conversion efficiency.

LED packages could also be classified in terms of the die structure. The MESA structure is the earliest form of LED dies that were widely used in low to medium power applications. The structure had two separate wire-bond connections for n-type and p-type contacts. Multiple wire-bonds, current crowding issues and complexity of the package has compelled the LED industry to shift towards other LED package architectures. The vertical LED structure was initially developed utilizing growth substrates such as SiC, which are also conductive. This would eliminate a wire-bond and simplify the package development process significantly. However, in modern vertical structure LEDs, growth substrate is removed using a laser lift-off process and a metallization layer evaporated onto the die. The flip-chip die structure has high photon extraction efficiency, since photons are extracted via the transparent substrate.

While different packages use different materials and have different package architectures, they share common failure mechanisms. However, the dominant failure mechanism may differ for different LED packages. Even though this dissertation would study only the vertical LED package, the methodologies and knowledge could be applied for other packages with caution.

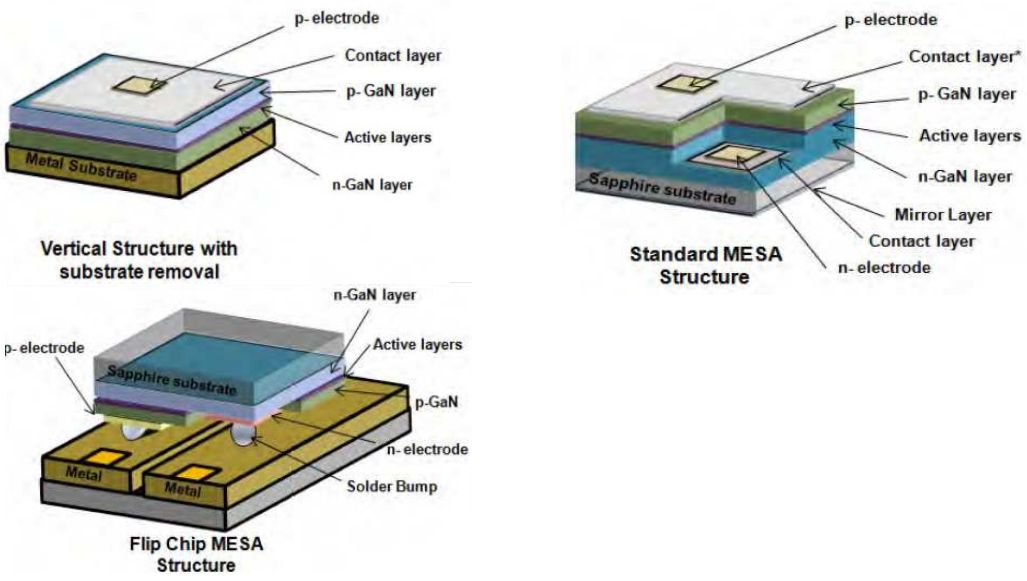


Figure 3. LED die structures [25]

1.4 Reliability of LED packages

One of the key value propositions highlighted by LED industry is its long life time. Therefore, reliability became a key point of interest for both high power LED package developers and their users. Early studies on InGaN blue LEDs (Nichia NLPB-500) showed that at continuous current operation, the optical emission intensity degrades over a period of time [26]. The degradation beyond 50% of initial value was defined as the parametric failure point. It was hypothesized that the degradation in the epoxy encapsulant is responsible for the intensity reduction. Subsequent studies that used the same LED package with a phosphor layer to produce white light showed that epoxy yellowing was the dominant failure mechanism, and the degradation rate depends on junction temperature and short wavelength radiation [27]. They observed that the light output follows an exponential decay.

The current reliability standard in LED industry defines life based on parametric failure. The alliance for solid-state illumination systems and technologies (ASSIST) recommended that life of an LED package is defined, for general illumination, as the point at which the light output reaches 70% of its initial value [28]. The recommendation provided for lumen maintenance measurement guidelines, also suggested using an appropriate decay rate model to project life time after 6000 hours of testing. The LED industries agreed on an approach to measure lumen maintenance (IES LM-80), and project the life of the LED package based on parametric failure (IES TM-21). The proposed projection methodology after evaluating different decay rate models for light output recommends exponential decay model for life time prediction. The research supports the exponential decay model only when the dominant failure mechanism is encapsulant degradation.

There is no industry wide standard to evaluate catastrophic failure of LED packages. Some LED package manufacturers perform accelerated life tests at temperatures, humidity, and current stress conditions stipulated by standards designed for semiconductor packages (MIL-STD, JEDEC) to capture and analyze catastrophic failure (JESD 22, JESD 22-A100D, JESD 22-A108D). These tests are typically qualification tests rather than life prediction tests.

The uncertainties of extrapolating the life of a device based on the information gathered through controlled accelerated stress conditions are high. Therefore, in applications that demands high reliability of system performance, prognostics and health monitoring (PHM) schemes would enable accurate prediction of end of life. The PHM schemes involve real time monitoring of stress conditions and device parameters to estimate remaining life of a device in an application [29].

In an LED package, electrical and thermal parameters can indicate the health of the device. Therefore, in this thesis both parameters were studied individually first to determine their usefulness in predicting failure. The changes in electrical and thermal parameters indicate different failure mechanisms. Therefore, in the final section both parameters were combined to develop single mode to predict LED package more reliably.

2 Electrical parameter study

2.1 Background

An LED package is a power conversion device where input electrical power is converted to thermal and optical power. The quality of electrical and thermal conduction path is an important consideration from the point of view of the device's performance. Electrical parameters such as, series resistance, ideality factor, reverse leakage current, and forward leakage current are potential indicators of the health of electrical paths. This chapter presents an equivalent electrical model for an LED package that will be used in the thesis for data analysis purposes. The theoretical basis for the model is discussed in detail. The primary failure mode of the electrical path is either open or short circuit failure. Therefore, the failure mechanisms that contribute to short and open circuit failures of LED packages are discussed in detail.

In order to develop a failure prediction model, these failure mechanisms need to be prioritized in terms of their susceptibility and severity. However, the available knowledge in literature is not sufficient to do such a prioritization for GaN based LEDs. In order to establish the root cause of failure that leads to open or short circuit failure, the changes that take place in electrical parameters up to the point of failure needs to be understood. When the root cause is established, a failure model that could predict the life time of an LED package when subjected to given stress conditions could be determined. The experimental results are used to calculate model parameters; these parameters are evaluated. When the life time and stress relationship is known, life estimation can be performed real-time in response to changes in stress conditions. Further, since the variation of electrical parameters up to point of failure is known, real-time failure detection criterion could be established.

This chapter discusses failure mechanisms presented in literature that could potentially lead to open or short circuit failure modes. The discussion is limited to failure mechanisms that cause a change in electrical parameters.

Details of the experiment, applied stress conditions, and data analysis are presented. The observed different phases of series resistance change are explained. A relationship between series resistance change, stress time, and stress condition is derived using electromigration and diffusion theory. The experimental results are compared with the derived relationship. This is the first time such an analysis has been performed for a long-term electrical contact degradation study for GaN-based LED packages.

2.2 Electrical model

A device physics based electrical model of an LED package is constructed for steady-state analysis purposes. The die is a semiconductor P-N junction sandwiched between two metal contacts. The metal-semiconductor contact is typically a Schottky barrier. However, in semiconductor applications the goal is to form a low resistance ohmic contact rather than a Schottkey contact. For the purpose of this model it is assumed that ohmic contacts are formed at p-GaN and n-GaN layers.

In addition to ohmic contact resistance mentioned above, the total resistance of the electrical path includes resistance of wire-bond, bond-wire resistance, resistance of solder layer, and copper trace resistance. All these resistances are connected in series with the diode. Therefore, this resistance is referred to as the series resistance in this dissertation. In addition to the series resistance there are parasitic resistances in the package that are several times larger than the series resistance. These parasitic resistances become comparable only when the applied voltage is less than the junction barrier voltage of the diode. The parasitic resistances are in parallel to the diode.

The main carrier transport mechanisms in diodes are diffusion, recombination, generation, and tunneling. According to Sah-Noyce-Shockley theory current through a P-N junction diode could be expressed as [30],

$$I = I_s(e^{\frac{qV}{nkT}} - 1). \qquad \text{equation A}$$

Where, I – forward current, I_s – saturation current, q – electron charge, n – ideality factor, k – Boltzman constant, T – temperature, and V – forward voltage.

In an ideal diode where diffusion is the only carrier transport mechanism, ideality factor is equal to one. The carrier injection into the depletion region would lead to recombination currents. The ideality factor is two for a diode with a trap energy level that is less than 10kT from the Fermi level [31], [32], [30]. However, in real life applications there are more than one trap levels in the energy band gap due to impurities of defects. Further, both diffusion and recombination carrier transport are there in a real diode. The relative significance of the two mechanisms may be different depending on the operating voltage and band gap of the material. The diodes with large band gap materials such as, GaN, GaAs, and recombination currents are significant. The deviation of ideality factor from unity is considered as an indication of the significance of recombination currents [33].

The ideality factor increase over time should suggest formation of traps, due to generation of defects or increase in impurity concentration in semiconductor material. The ideality factor analysis is performed at low current regions where, the current-voltage characteristic of the package is not limited due to package series resistance. Therefore,

ideality factor analysis enables separation of semiconductor degradation from electrical contact degradation in a package.

The electrical characterization studies on InGaN devices have shown a high device ideality factor that cannot be explained using the Sah-Noyce-Shockley theory [30], [34], [35]. Therefore, it is hypothesized that the electrical transport in an LED device is a combination of tunneling, diffusion, and recombination currents [31], [36]. The current-voltage relationship for the tunneling diode could be stated as [32],

$$I = C_1(e^{\left(\frac{qV}{E_T}\right)}\text{-}1). \qquad \text{equation B}$$

Where, C_1 – constant dependent on built in potential and density of impurity traps, E_T - energy constant, q – electron charge, V – voltage , and I – current.

A typical forward biased current (I)-voltage (V) characteristic of an LED package is given in Figure 4. There are four distinct regions in the current-voltage characteristics, where different resistances and carrier transport mechanisms dominates. In region 1, at low forward bias, the leakage current flows via the high parallel resistance. In region 2, the junction is not forward biased, but there is current flow due to space charge recombination, and tunneling. At this region the exponential relationship between the current-voltage exists but, the ideality factors are greater than 2. Therefore, equation B is more appropriate to express I-V relationship in this region. In region 3, the diode is forward biased and the carrier transport is dominated by tunneling and recombination. Therefore, ideality factors are closer to 2 and equation A is applicable. At high currents, region 4, voltage drop across the series resistance becomes significant [33], [37].

In this study an equivalent electrical model that is based on device physics is proposed in Figure 5. The three parallel diodes represent the three current transport mechanisms; diffusion, recombination, and tunneling. Each would have its own turn on voltage, as they become dominant at different voltage regions.

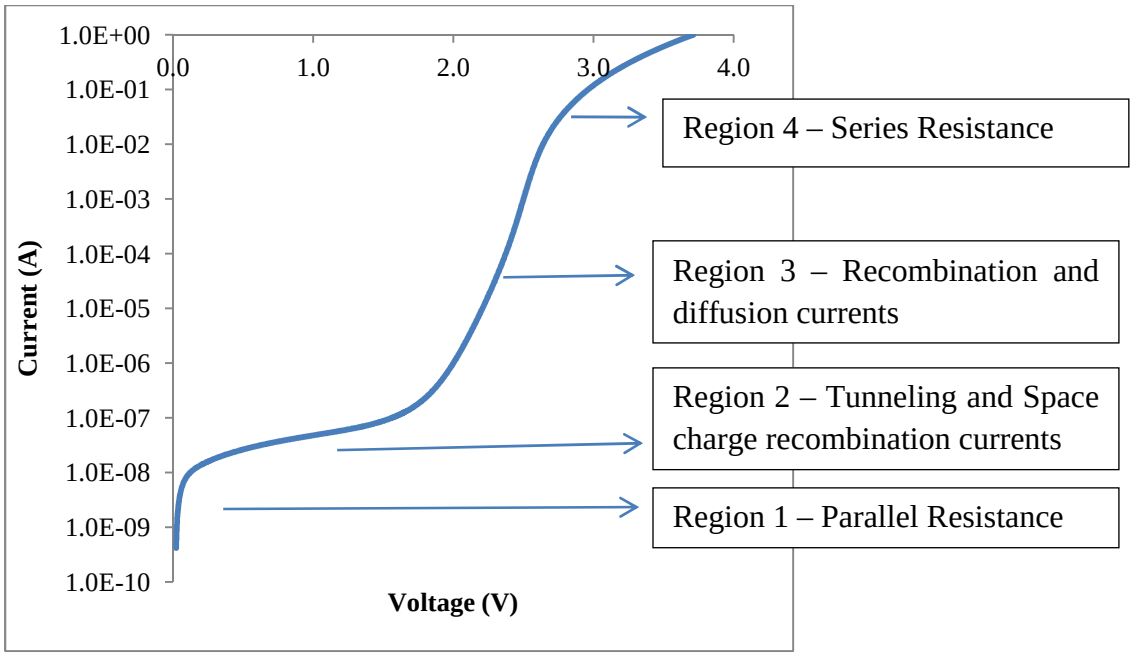


Figure 4. Forward biased current-voltage characteristics of an LED package

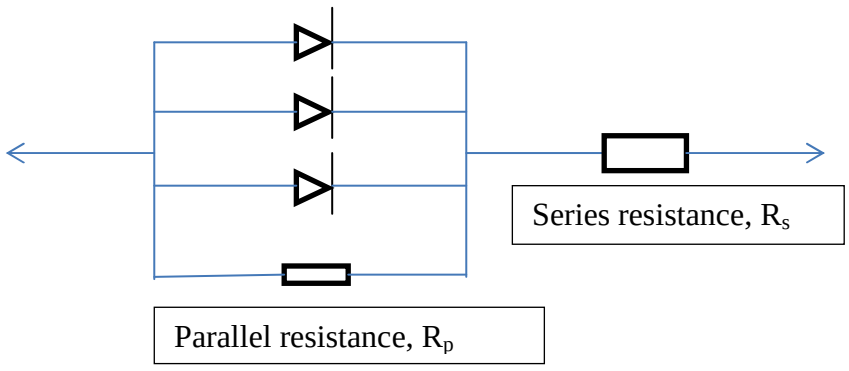


Figure 5. Electrical model

2.2.1 Temperature characterization of electrical parameters

The current-voltage characteristics of InGaN/GaN devices are temperature dependent as shown in Figure 6. The resistance of semiconductors decrease with temperature due to activation of donors and acceptors outside the active region [32]. Thermal activation increases the population of electrons/holes that crosses the metal/semiconductor barrier. Therefore, effective contact resistance would also decrease. However, the electrical resistances of metals increase with temperature due to phonon scattering phenomenon [38].

The temperature characterization of electrical parameters was performed for the LED package type used in this study (InGaN-based vertical structure LED). The characterization was performed by measuring I-V characteristics at different temperatures. The measurement protocol described in section 2.4.6 was followed when extracting I-V characteristics.

The package consists of both metals and semiconductors. The temperature coefficient for resistance for metals is positive, but very small. However, the experimental evidence shown in Figure 7 shows a negative temperature coefficient for resistance. This suggests that the resistance change is dominated by the semiconductor. The thermal activation energy for resistance change is 105meV.

Electrical characterization of the LED package at different temperatures showed that ideality factor at region 3 in Figure 4, decreased with temperature. At high temperatures the contribution of thermal diffusion to overall current transport increases. Which means the behavior of diode gets closer to an ideal diode. Therefore, ideality factor should get closer to 1, as shown in Figure 8. The thermal activation energy of this mechanism is 20meV. This is the activation energy of Si, a commonly used donor in n-GaN device fabrication [39].

The ideality factors of region 2 in Figure 4 remain constant till 323K and then decreases with temperature. At region 2, current transport is dominated by tunneling currents which are insensitive to temperatures. At higher temperatures, space charge recombination near the ohmic contacts increases, thereby reducing the ideality factor. The thermal activation energy is 170meV, which is the activation energy of Mg, a commonly used acceptor in the P-GaN region [40].

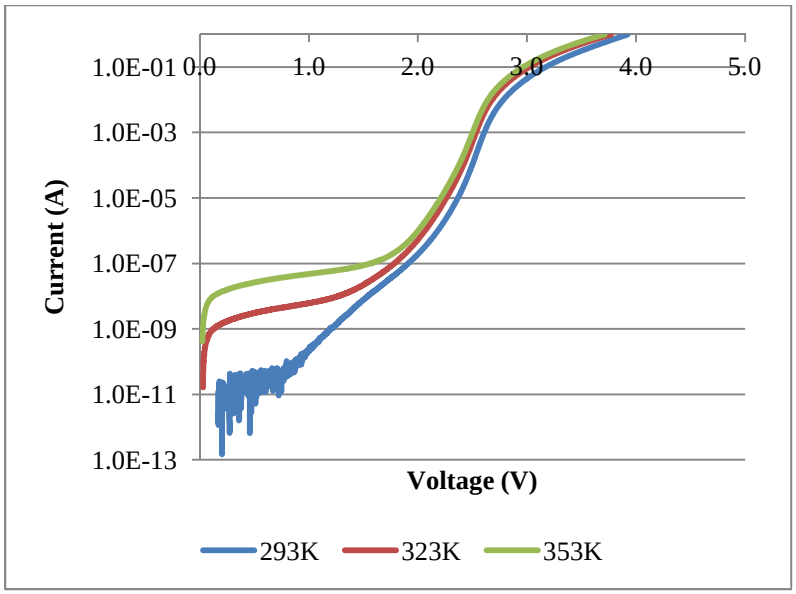


Figure 6. The variation of forward current-voltage characteristics of GaN-based LED package

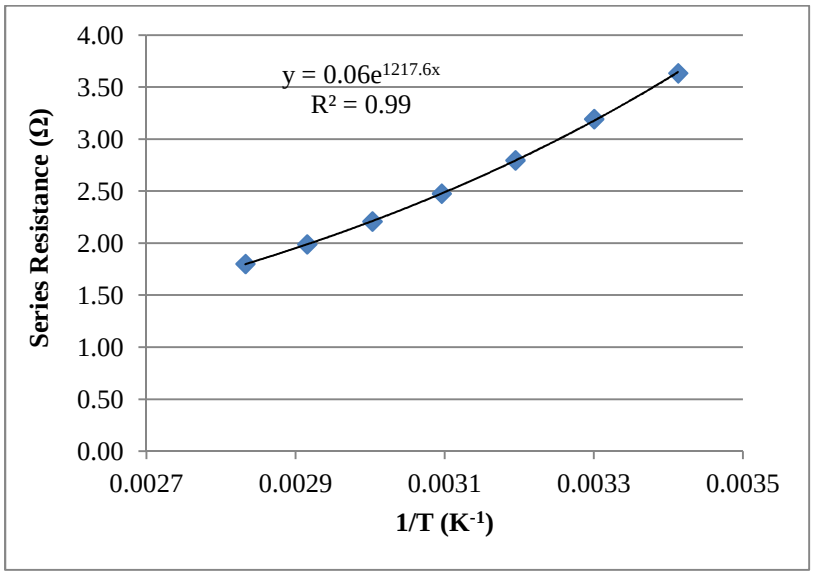


Figure 7. Series resistance change with temperature of GaN-based LED package

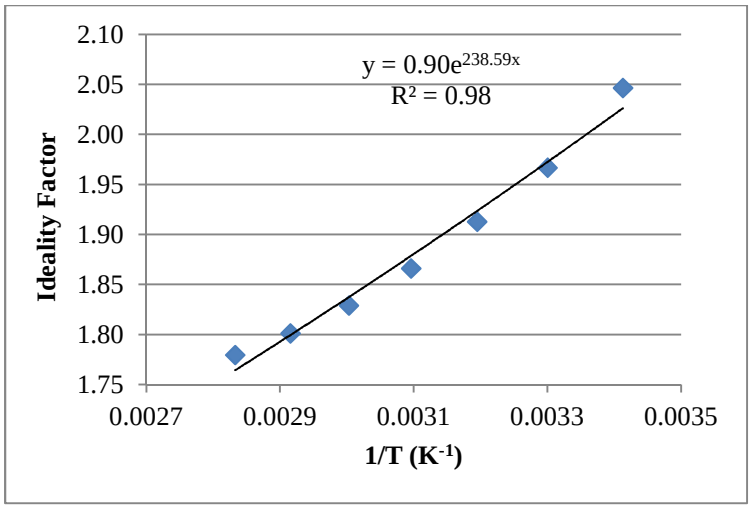


Figure 8. Ideality factor (Region 3) change with temperature of GaN-based LED package

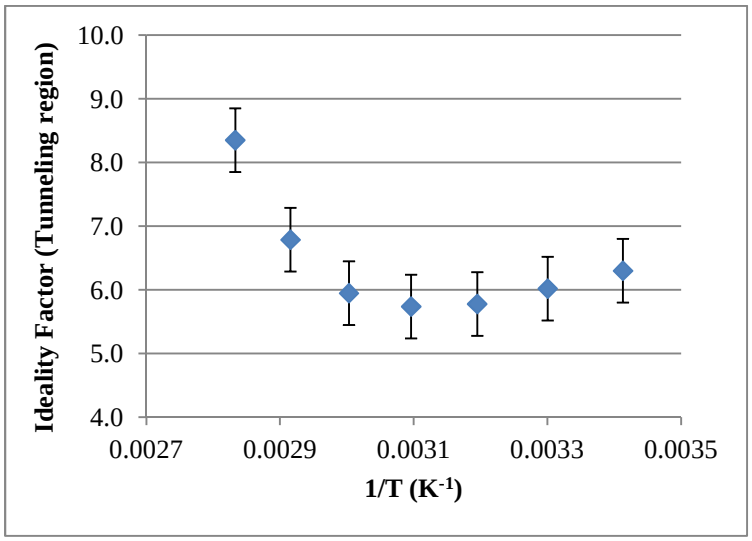


Figure 9. Ideality factor (Region 2) change with temperature of GaN-based LED package

2.3 Failure mechanisms

There are two possible catastrophic failure modes in an LED package, open circuit and short circuit. There are numerous probable failure mechanisms that contribute towards these failure modes. The focus of this dissertation is the catastrophic failure modes, and failure mechanisms that could be detected by measuring electrical and thermal parameters.

2.3.1 Electromigration

Electromigration is the mass flow process that occurs in a conductor due to momentum transfer from moving electrons to ions in a lattice [41]. Any conductor at a given temperature would have random self-diffusion of ions. The electromigration makes this random process directional. The directionality is determined by the balance of electric field induced force, and electron wind force due to momentum exchange, on ions [41], [42], [43]. This process depends on the current density and temperature. The simplified Blacks' equation that provides a relationship between median time to failure (MTTF) due to electromigration, and stress conditions is given below.

$$MTTF = AJ^{-n}\exp\left(\frac{E_a}{kT}\right)$$

equation C

Where, A- material and geometry factor, E_a- activation energy, k – Boltzman constant, T- temperature, and J - current density.

Past studies have identified electromigration in metal contacts as the main failure mechanism in integrated circuit (IC) packages [42], [43], [44], [45], [46], [47], [48], [49], [50]. Electromigration creates non-uniform atomic flux distribution in a conductor that leads to formation of voids and hillocks. The void in a conductor increases its resistance [44], [46], [47], [48]. Therefore, formation of voids would lead to high localized current densities and increase in temperatures. This would lead to acceleration of electromigration within that locality. The mass accumulation at given location create short circuits between conductors. In the case of semiconductor-metal contacts the mass accumulation transport metals to semiconductor surface. These metals could then diffuse into the semiconductor material, especially if there are vacancies in semiconductor. In the case of GaN these vacancies are provided by large number of dislocations [51], [52].

The mass flow due to electromigration creates localized stress gradients which in turn creates a back flow of atoms, leading to partial or complete healing of voids [53]. Belch introduced the critical length concept, where for electromigration to be an effective failure mechanism, the length of the conductor should be greater than the critical length. However he didn't observe the back flow phenomenon in gold contacts. On the contrary other researchers showed that there is back flow of atoms in gold contacts and they measured critical product factors (critical length x current density) that range from 600 to 3000A/cm [48], [54].

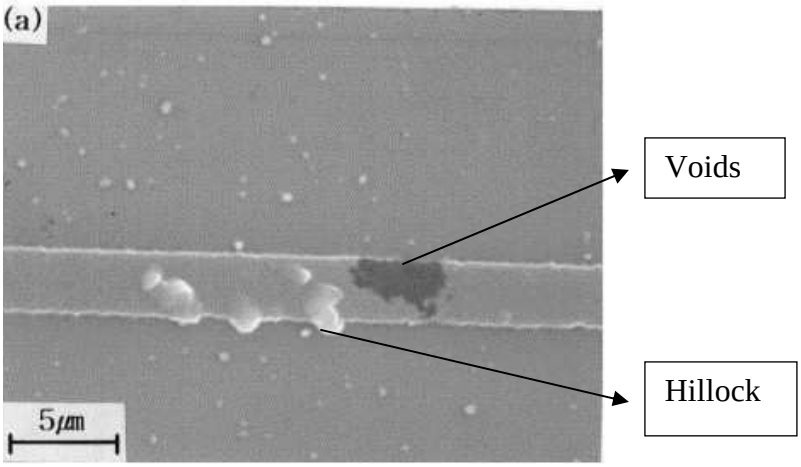


Figure 10. Void and hillock formation in Aluminum thin film due to electromigration at 200^0C [55]

The migration of metal atoms along defects of semiconductor materials was hypothesized as a catastrophic failure mechanism for LED packages [56], [57], [58], [59], [60], [61], [62]. Life time studies on InGaN indicator type LEDs with Au/Ni contacts showed that the life time of the device depends on the current density. The study showed an empirical relationship between device life time (t_f) and current density (I) in the form of,

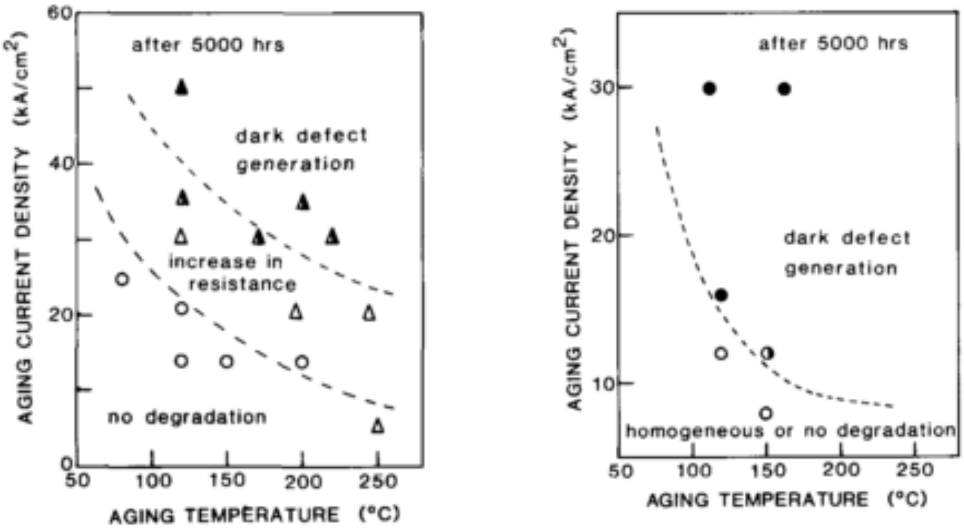
$$t_f = \frac{C}{I^n}.$$

Where, C is a constant, and n is the current exponent that is closer to 2 when junction heating is negligible [56].

In this study junction or case temperature was not controlled. The only evidence authors present to support their hypothesis that contact electromigration was the failure mechanism is the empirical relationship given above. Since they did not control junction temperature at different current densities, the above relationship is not similar to Blacks' equation. The measured current exponent values are far greater than the reported values for Au or Ni contacts, which may have been due to non-separation of current and heating effect. Another study that performed failure analysis on indicator type GaN LEDs that were subjected to short high current pulses (100ns/1kHz, 1.5A) observed a low resistive contact path from p-contact to n-type side via junction [57], [58]. They used electron beam induced current imaging (EBIC) to observe this current path. However, the study was not conclusive as to whether the short circuit current path was along an existing defect or a defect formed due to current stress. They also observed an increase in forward and reverse leakage current.

Lifetime studies on InGaAsP/InP LEDs and laser diodes showed formation and expansion of dark spots and dark lines as the fundamental failure mechanism [61], [62], [63], [64], [65]. The dark spot formation was attributed either to metal migration or precipitation of host atoms. The Au migration from P-contact is identified as the dominant factor that contributes towards formation of dark spots in the active region [61], [65]. The number and size of dark spots expand significantly with aging, and a sudden drop in the light output would occur, leading to catastrophic failure of the device. In this case catastrophic failure occurs due to a junction short-circuit. The stress factors that accelerated this failure mechanism is temperature and current density [66].

The diffusion process that leads to dark spot formation in active region also degrades the metal electrodes. This leads to an increase in series resistance. The open and partially closed triangles in Figure 11 (a), represents the degradation of LEDs due to an increase in series resistance. These LED samples eventually fail, after a gradual increase in series resistance. This is explained as, inter diffusion of Ga, In, and Ti particles from Ti/Pt/Au ohmic contact, that form a depletion region with a higher series and thermal resistance [66]. In Figure 11 (b), open and partial circles indicates LEDs that showed an increase in series resistance prior to failure. The diffusion of Au atoms from AuZn electrode leads to formation of high resistance alloys. This study shows that diffusion of Au in to the active region takes a finite amount of time (at moderate stress conditions) and during that time period series resistance increase.



(a) (b)

Figure 11. The current and temperature induced degradation of InGaAsP LEDs with Ti/Pt/Au (a) AuZn (b) p-electrodes after 5000 hours [66]

2.3.2 Dopant compensation at P-GaN layer

A passivation layer is deposited on dies using PECVD (plasma enhanced chemical vapor deposition) technology, for encapsulation and for reduction of surface recombination currents [67], [68]. If a hydrogen rich passivation layer is used, at high temperatures hydrogen in the passivation layer interacts with Mg dopant in the P-GaN layer. The formation of Mg-H complexes causes p-dopant compensation, reducing the carriers available for recombination. The formation of $Mg\text{-}H_2$ metastable complexes is a thermally activated process [67], [69]. This failure mechanism leads to worsening of ohmic properties at the GaN/metal interface. This is due to the increase in Schottky potential barrier as a result of reduction in the acceptor concentration in the p-type region [70]. As a result of dopant compensation, series resistance of the diode increases. This increase is due to an increase in ohmic contact resistance and not due to the increase in p-GaN sheet resistance. The increase in contact resistance at the GaN/metal interface would lead to current crowding. Due to the above discussed failure mechanism, when subjected to thermal stress, the forward voltage of a passivated InGaN die increased with aging [67], [68].

2.3.3 Wire-bond failure

The wire-bond distributes current to the semiconductor. The application of bonding pressure to establish a smooth electrical connection during the wire bonding process could damage the die. On the other hand inadequate wire-bond strength would lead to high contact resistance, thermal resistance, and uneven distribution of current across the chip. Contamination of chip surface with adhesives during assembly also hinders good electrode bonding [71], [72].

High junction temperatures, combined with temperature cycling, and thermal expansion coefficient (CTE) mismatch between encapsulation materials, die, and wire-bond causes significant thermo-mechanical stresses on the bonding interface. This in turn cause fatigue cracks that will lead to catastrophic failure [71], [73]. The large area cracks formed due to thermal cycling will propagate from the inner bonding pads to the active region of the die [72]. Current pulsing can cause flexing of wire-bonds that leads to second order fatigue failures [74]. Some plastic encapsulation materials used in semiconductor packaging have flame retardant chemical compounds that out-gas at high temperatures and form intermetallic compounds (IMC) at Al/Au interconnections. The formation of IMC would lead to reduction of ball-bond shear strength and cause failure [75].

2.3.4 Solder joint failure

The solder joint provides an electrical connection and mechanical bonding in LED packages. The solder joint in a package is subjected to thermal-fatigue induced strains due to CTE mismatch between the die and the substrate. The creep and plastic strain causes metal fatigue, which leads to solder joint failure. There are several solder joint life prediction models based on the strain range, accumulated creep strain, and strain rate [76], [77], [78], [79]. Also during aging, IMCs form in the solder pad due to diffusion of metals. The IMC formation leads to formation of micro voids between the IMC and bulk solder that would eventually lead to failure [80]. In a package there could be an array of solder joints, and not all of them fail simultaneously. However, thermal simulations showed that even a few solder bump defects in a flip-chip package could cause non-homogenous temperature distribution in the chip [81].

Solder joint failure in electronic packages are detected using resistance change. Studies have reported a correlation with applied strain and resistance change of solder joints [82], [83]. To determine the reliability of solder joints, the electronics packaging industry follows standards such as IPC-SM-785 (November 1992), IPC-9701 (January 2002), JESD22-B111 (July 2003), IPC/JEDEC-9702 (June 2004). Some standards define a failure criterion as a percentage increase from initial resistance. Solder joints go through intermittent failure that causes electrical discontinuities before eventual open circuit breakdown. Therefore, some standards require detection of resistance spikes, their frequency, and spike width to detect solder joint failure.

Thermal cycling generates fatigue cracks in the solder joint. Under mild thermo-mechanical stress conditions these cracks remain stable, but there is a consistent increase in resistance with time. However, the amount of increase in resistance depends on the cycling conditions. When cracks are formed, solder joints show non-metallic tunneling behavior that facilitate electron transport [84], [85]. The time it takes for cracks to open depends on stress conditions and environmental conditions, such as humidity [84]. It is also important to estimate the temperature coefficient of resistance especially when measuring small resistances, to ensure resistance increase is not due to temperature [84].

The following scenarios could occur when solder joints are subjected to cyclical thermal stress. The resistance would increase gradually up to a certain point and rapidly increase thereafter. In this case it is reasonable to set a threshold as a failure criterion. Alternatively, resistance would increase initially then stabilize before a sudden increase that leads to open circuit failure. This is possible in mild thermo-mechanical stress conditions. In this scenario, it is hard to define a failure criterion based on a threshold for the resistance. In these cases, resistance spikes (magnitude, frequency & spike width) would indicate failure [83], [84].

2.3.5 Defect generation & mobility

In spite of its high threading dislocation density, GaN devices are stable and have high quantum efficiency [86]. This is attributed to lower mobility and electrical inactivity of its dislocations. However, at high temperatures induced by high currents, the glide motion of dislocations is triggered [87]. High contact resistivity, localized high current densities, and non-radiative recombination close to defects can cause high localized temperatures that increase defect mobility [73], [88]. Even when LEDs are subjected to low currents, mobility of defects is possible due to uneven current distribution [89].

The quantum efficiency of the device is reduced by mobility of defects. The strains in the material system due to the motion of defects, form V-defects in the p-GaN that behave as electrically active non-radiative recombination centers [90]. The degradation studies on III-V compounds showed formation of dark line and point defects on the active region of the device. It was hypothesized that these formations are due to movement of defects that create non-radiative recombination centers [91].

An optical power degradation model that assumes that the primary reason for degradation is the electron-hole non-radiative recombination on a defect point, showed that light output has an exponential degradation in the short term, and inverse time dependence in the long run [92]. Another study on AlInGaN LEDs showed that there is a relationship between the initial reverse bias leakage current and degradation rate. In this study it was hypothesized that reverse leakage current is correlated with the number of defects in the material. Therefore, reverse bias leakage current was suggested as a good indicator for initial screening of LEDs [90]. However, it is only the movement of defects in the active region of the device that causes an optical power reduction. The movements of defects in the cladding layers increase reverse leakage currents, but don't affect device performance. The presence of defects in the device also facilitate tunneling; therefore, forward leakage currents increase with aging [93].

2.3.6 Passivation/dielectric layer breakdown

Passivation is performed on the LED die to,

- reduce surface leakage currents due to dangling bonds.
- act as a die-electric/insulating layer between ohmic contacts, and
- Treat the dangling bonds formed during chemical etching process

The commonly used passivation layers are SiO_x and SiN_x. The SiN_x layer is preferred in modern high power packages due to its high breakdown strength. The breakdown of the passivation layer is a potential reliability concern for flip-chip and thin-film vertical LED

package structures. In these structures both p-type and n-type contacts are provided from the same direction and passivation layer is used as the insulation layer to isolate the two contacts.

The breakdown of passivation/di-electric layer is a reliability issue in SiC based high power devices (ex: MESFET & SITs). The breakdown of passivation layer depends on the temperature and applied electric fields. In these applications the die-electric layer is subjected to electric fields in the order of (1-10MV/cm). The failures of die-electric layers were observed at electric fields greater than 5MV/cm and at temperatures greater than 250^0C [94], [95], [96]. The die-electric layer degradation leads to an increase in device leakage currents.

However, there is no known study that reported the breakdown of dielectric/passivation layer of LEDs. This may well be due to the fact that in LED packages operating temperatures and electric fields are lower than the thresholds discussed above. The reliability study that stressed LED at 250^0C saw an increase in contact resistance but didn't observe a breakdown in passivation that led to short circuit failure [68].

2.3.7 Conductive filament formation

In applications, LED packages are attached to a printed circuit board (PCB). The PCB also contains conductors for electrical contact and insulation between these conductors to prevent short circuit of negative and positive terminals. The current densities and thermal densities are comparatively small in these layers to induce mechanisms such as electromigration. However, conductive filament formation between the negative and positive pad is a potential device failure mechanism that is observed in PCBs used in electronic circuits [43], [97].

This filament formation process is referred to as electrolytic electromigration. Unlike the solid state electromigration that was discussed in section 2.3.1, this process doesn't require high temperatures or current densities [43]. The key factor that facilitates this phenomenon is the formation of a path between two conducting traces [97]. This path creation process could occur due to fatigue, moisture absorption, impurities such as dust, or fabrication defects. Once the path is created Cu ions migrate through an electric-chemical process, creating a short circuit. The insulation resistances decreases with aging due to the formation of a low resistance current path and eventually cause short circuit failure.

2.3.8 Summary: Failure mechanisms

The failure mechanisms that could lead to open and short circuit failures in an LED packages discussed in the above sections are summarized in the Table 1.

Table 1. Summary of failure mechanisms that affects electrical parameters

Failure mechanism	Failure mode	Electrical parameter change	Stress conditions
Metal impurity diffusion into active region	Junction short-circuit failure	Series resistance decrease Ideality factor increase Reverse leakage current increase	Current density Temperature
Electromigration leads to void formation in contact metallization	Open circuit failure	Series resistance increase	Current density Temperature
Dopant compensation	Open circuit failure (Joule heating)	Series resistance increase	Temperature
Wire-bond fatigue failure	Open circuit	Series resistance increase	Temperature Thermo-mechanical stress due to CTE mismatch
Solder joint fatigue failure	Open circuit	Series resistance increase (resistance spikes due to intermittent connections)	Temperature Thermo-mechanical stress due to CTE mismatch
Defect generation and mobility	Short circuit	Reverse leakage current increase Ideality factor increase	Temperature Current
Conductive filament formation at PCB	Short circuit	Series resistance decrease Reverse leakage current increase	Humidity Electric field External contaminants
Die-electric passivation layer breakdown	Short circuit	Reverse leakage current increase Series resistance decrease	Electric field Temperature

It is evident from the failure mechanisms reported in Table 1, that almost all failure mechanisms cause a change in package series resistance. Therefore, it's a promising parameter to detect failure. Further, it is relatively easier to measure in an in-situ measurement environment. Therefore, a systematic study of the series resistance of an LED package with aging and stress conditions would yield valuable information with regard to the health of an LED package.

Reliability studies on InGaN based LED packages showed an increase in forward voltage and series resistance with aging [98], [99], [100], [101], [102]. In these studies it was hypothesized that the increase in series resistance was due to degradation in the ohmic contact. One such study performed a high temperature storage test on LED packages by storing them at 180^0C-230^0C [100], [102]. They observed an increase in forward voltage at a current of 400mA as a function of storage time, as shown in Figure 12. However, they didn't see a correlation between light output change and series resistance change. The failure criterion used was 70% reduction in light output, as opposed to any electrical parameter change. It was hypothesized that the dominant failure mechanism is package and phosphor degradation, and the calculated activation energy of 1.5eV associated with it.

The series resistance of InGaN flip-chip LED packages, that were subjected to stress conditions of, 100^0C temperature, and 50-200mA current for 600h increased with aging [101]. It was hypothesized that the degradation occurred at the p-GaN semiconductor layer rather than on Ag metal contact. However, authors didn't report whether the current density had any impact on the series resistance increase. The aging study that subjected LED packages for 350mA current stress, and 85^0C ambient temperature stress, saw an increase in series resistance after 4000h of aging [98]. The initial reduction in series resistance was attributed to annealing effects. They also observed a large monotonic increase in tunneling currents during aging.

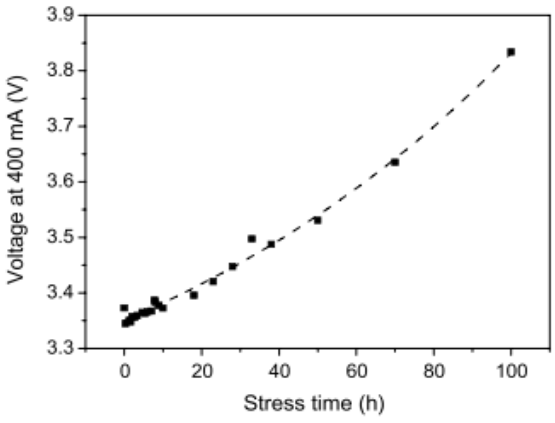


Figure 12. Forward voltage change with stress time for an LED package stored at 200^0C [100]

2.4 Knowledge gap

Even-though there are studies that reported an increase in series resistance with aging when subjected to current and temperature stresses, none of them monitored these parameters up to the point of catastrophic failure. The series resistance increase was not correlated to any failure mechanism. It is also not known whether the series resistance change rate has any temperature or current dependence. All of this information is important to develop a failure prediction model for electrical contact failure.

The main focus of the reliability studies discussed in the previous sections for InGaN LEDs is their parametric failure. Electrical parameters were monitored to explain the degradation mechanism that causes parametric failure. In these studies there was no clear evidence to suggest that parametric failure was caused by degradation of electrical contacts. Hypotheses that suggested degradation mechanisms such as electromigration, and ohmic contact degradation are responsible for series resistance increase were put forward by researchers. However, none of these hypotheses were validated.

In this thesis study the variation of series resistance of high power LED will be monitored and analyzed up to the point of catastrophic failure under different steady state temperature and current stress conditions. The study will investigate the degradation kinetics of electrical contacts by analyzing the systematic and irreversible change in series resistance under various stress conditions. This will be the first study that will analyze the long-term change in series resistance due to degradation of electrical contacts of InGaN based LED packages. Analysis of other electrical parameters such as, ideality factor, and reverse leakage current can provide clues to the dominant failure mechanisms.

2.5 Hypotheses

The evidence discussed in detail in the sections above can be used to formulate following hypotheses.

If an InGaN based LED package is subjected to thermal stress, by increasing the junction temperature, then the irreversible rate of change of series resistance increases.

There are no known studies that have developed a relationship between series resistance change rate and temperature. However, a careful analysis of failure mechanisms listed in Table 1, shows that failure mechanisms such as electromigration, dopant compensation, solder joint failure, wire-bond failure, and defect generation are activated by temperature. Further, many of these contact degradation mechanisms rely on diffusion, and therefore, on temperature. The junction temperature of an LED package is a good indicator of temperatures at the vicinity of the die, where many of the contact failures occur.

If an InGaN based LED package is subjected to current stress, by increasing the current density, then the irreversible rate of change of series resistance increases.

The evidence presented in literature review shows that failure mechanisms such as, electromigration, defect generation and mobility are accelerated by the current density. In context of the above hypotheses, the following terms are defined below.

- LED package refers to a single-die LED package. The definition of LED package is provided in section 1.1.
- Junction temperature refers to junction temperatures from 140^0C to 175^0C.
- Current density refers to current densities from 236A/cm^2 to 355A/cm^2. Current density is calculated as, operating current over die area. The above current densities correspond to operating currents from 1A-1.5A.
- Series resistance is extracted from the current-voltage characteristics of the LED package as explained in section 2.7.1.

2.6 Experiment Design

There are two parts to the experiment. The two part design was adopted to separate the effect of temperature induced stress and current induced stress. The first part will investigate the impact of junction temperature on catastrophic failure and series resistance. This will help to establish the activation energy of the dominant failure mechanism. The LED packages were tested under three different junction temperature conditions. Junction temperature is a good indicator of operating temperature of electrical contacts that are closer to the die. The three junction temperature conditions chosen were 140^0C, 150^0C and 175^0C. These temperatures were chosen so that the degradation of the package is accelerated. The maximum rated junction temperature for this package was 145^0C. The independent, dependent, and extraneous variables for this part of the study are as given below.

Independent variables

- Junction temperature – The junction temperature (T_j) measurement procedure is explained in the thermal characterization section. The T_j of the device was controlled by varying the case temperature.
- Stress time

Dependent variable

- Time to catastrophic failure (Open or short circuit failure)
- Series resistance

Extraneous variables

- The operating current – the operating current was kept constant at 1A using a constant current LED driver.
- LED packages are mounted in same orientation
- Humidity – The humidity of the ambient air surrounding the package was not controlled during the study. The impact of hygro-mechanical stresses on LED packages have been studied [103]. The study showed that the impact of thermo-mechanical stresses is larger when compared to hygro-mechanical stresses. Further, many of the materials used in LED packages don't absorb water, therefore is not susceptible to hygro-mechanical stresses. Therefore, it is anticipated that humidity would not have significant impact on failure.

The second part of the study investigates the impact of current density on catastrophic failure and series resistance change. This would help to identify the contribution of current induced strain on the LED package. Three current stress conditions, 1A, 1.25A, and 1.5A were used. The rated continuous direct current for this package is 750mA. The junction temperature would remain constant at 150^0C for all the current stress conditions. The independent, dependent, and extraneous variables for the study are given below.

Independent

- Current density – The current density to the LED package was changed by changing the applied current (1A-1.5A). The dimensions of the LED die are identical for all cases.
- Stress time

Dependent variable

- Catastrophic failure time
- Series resistance

Extraneous variable

- Junction temperature – The T_j of the LED packages was kept constant at 150^0C for all cases, by applying heat sinking and forced cooling.
- The mounting orientation – LED packages were mounted at the same orientation.
- Humidity – Humidity was not controlled during the study.

2.6.1 Materials

Phosphor converted white, InGaN single die LED package was used for the aging study. The LED package is a commercially available product, and schematic of the package is given in Figure 13. The LED package has a vertical structure, with the die attached to a conductive silicon submount. The submount is attached to a copper coated ceramic substrate. The die-submount attachment is performed using $Au_{80}Sn_{20}$ solder. The submount-substrate attachment is performed using Sn-Ag-Cu solder compound. A gold wire with a diameter of 35µm is used to conduct current to the die. The ohmic contact at the p-GaN layer is formed using an Au/Ni metallization layer. There is a patterned Au/Ni metal trace on the cathode side that provides the electrical contact to the n-GaN layer. A SiN_x passivation layer helps to minimize the surface leakage currents, and provide a die-electric barrier between electrical contacts. A phosphor is coated on every single element inside the package. The package has a silicone encapsulant held by a metal ring that is attached to the ceramic using epoxy. The ceramic layer has three sections: anode, cathode and heat sink. There are Cu plated vials in the ceramic to conduct heat from the substrate to MCPCB. The ceramic is attached to the MCPCB using solder.

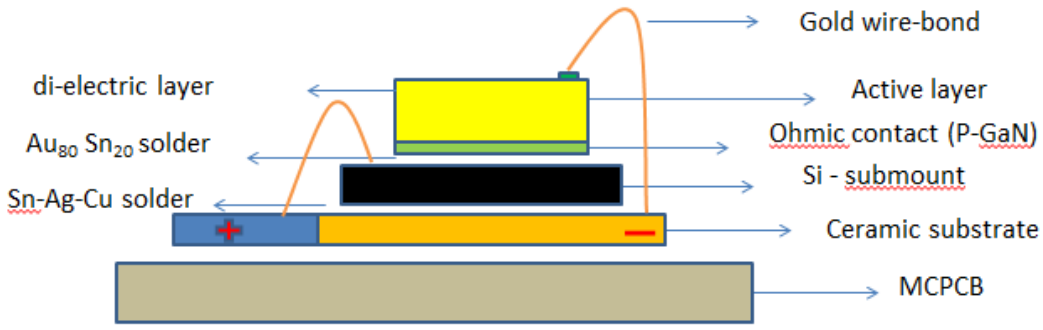


Figure 13. Schematic of the LED package

The die used in the LED package is EZ700, manufactured by CREE Inc. in USA. The maximum operating ratings of the die is given in the table below.

Table 2. The absolute product ratings as given by the manufacturer [104]

Parameter	Rating
The maximum DC current	750mA
The maximum peak current	1000mA
The maximum junction temperature	145^0C
The maximum Reverse voltage	5V
Operating case temperature range	-40^0C – 100^0C
Typical forward voltage at 350mA	3.5V
The reverse biased current at -5V	2µA

2.6.2 Experiment set-up

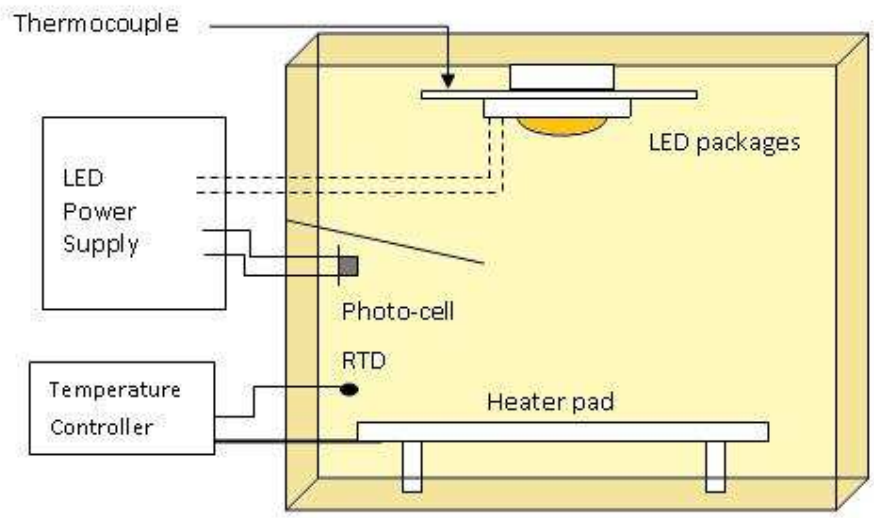


Figure 14. Schematic of the LED life test box

A schematic of the experiment set up used for the aging study is shown in Figure 14. The LED package was mounted using mechanical screws, inside a wooden box, painted in white. The MCPCB does not touch the wooden surface. The temperature inside the box is controlled using a heater pad, RTD (100Ω platinum), and a temperature controller (Minco – CT325 miniature DC). The temperature controller uses the RTD input as the feed-back and regulates the current to the heater pad based on the set point. The regulation of box temperature, enable the control of both case temperature, and junction temperature.

The LED packages are powered using a constant current driver with an output current of 1A (Advanced LED driver). The output current of the driver, is measured using a current sense resistor (Ohmite, 0.1Ω, 1%, 4.5W). The light output is measured using a photo-detector which is covered using a baffle for direct light incidence. The silicone photodiode (Hamamatsu S1226) has the highest sensitivity at 720nm, and is used for relative light output measurement. The case temperature of the LED package is measured using a T-type thermocouple. The voltage, current, case temperature, box temperature, and photo detector readings are recorded at every one hour, during the study. The data is acquired using a DAQ (Agilent 34970A), and a data acquisition program in Labview (National Instruments).

2.6.3 Experiment protocol

LED packages used in this study were pre-burned for an hour to filter out any infant mortalities. Five samples were prepared for each test condition. Each sample was electrically and thermally characterized prior to the aging study. A T-type thermocouple was attached on the MCPCB using solder. The attachment point was closer to the center of the ceramic substrate for case temperature measurement. To account for individual differences in thermal resistance values, thermal resistance values of all LED packages were measured at conditions that are similar to their respective aging environment. The procedure for thermal characterization is explained in section 3.3.1. The case temperature was controlled within $\pm 2^0$C to maintain junction temperature at the intended value. Periodic measurements of thermal resistance were performed during the study to ensure that T_j is maintained within $\pm 2^0$C of the set value.

In addition to thermal characterization, the current-voltage characteristics of all samples were extracted prior to the reliability study. The details of the electrical characterization are given in section 2.6.4. The Microscopic images of all samples were acquired before the test.

After electrical and thermal characterizations each sample was mounted inside the wooden box shown in Figure 14, and was subjected to their respective stress conditions. The samples that were subjected to 1.25A and 1.5A stress conditions required forced cooling, to maintain their junction temperature at 150^0C. They were mounted on to a heat sink using mechanical screws and a fan with a regulator was used to provide the required air velocity. The voltage, current, and temperature data were monitored for all LED packages every hour. The current-voltage (I-V) characteristics were extracted off-line from LED packages, periodically. The frequency of I-V analysis depends on the severity of the stress conditions, with a view of obtaining the most number of series resistance data points, before failure. The electrical characterizations were performed at 25^0C. This is the cold plate temperature of the thermoelectric cooler. After failure, the sample was initially checked to identify the failure mode (short circuit or open circuit). Then each failed sample was put in sealed plastic bag for failure analysis.

2.6.4 Electrical characterization

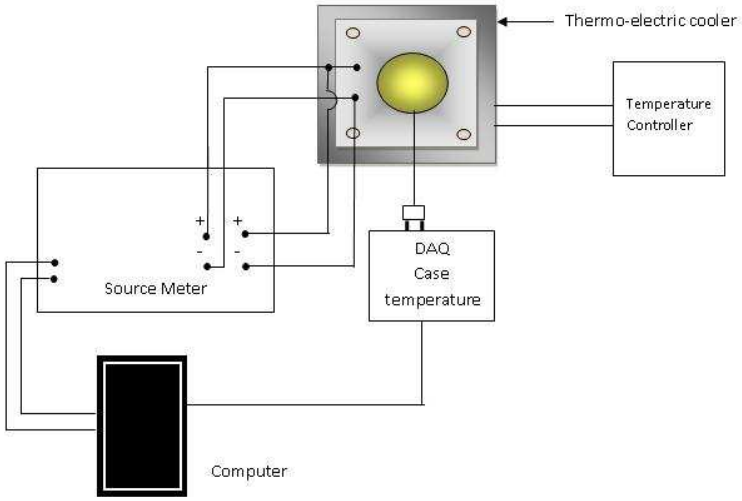


Figure 15. Electrical characterization experimental set up

Two types of electrical characterizations were performed. The current-voltage (I-V) characterizations from the beginning of the aging study till its failure. The current-voltage-temperature (I-V-T) characteristics were extracted before aging. A schematic diagram of the measurement setup used for current-voltage (I-V) measurements is given in Figure 15.

A T-type (5SRTC-TT-T-30-36) thermocouple was attached at a point closer to the ceramic substrate, using a solder. The LED package was attached to the thermoelectric cooler using mechanical screws. The cold plate temperature of the thermoelectric cooler (Arroyo Instruments, LED/laser mounts-226), was controlled by a temperature controller. The T-type thermocouple was connected to a data acquisition unit. The lead wires coming out from the LED was connected to a source measurement unit (Keithly-2430) for electrical characterization purposes. Four-wire measurements were performed to eliminate the effect of lead wire resistance in the measurement. The source measurement unit, data acquisition unit (Agilent 39470A), and temperature controller is connected to a computer through a GPIB interface and is controlled using LabView-2010, national instruments software.

The LED package was allowed to thermally stabilize before initiating the I-V sweep. The thermal stability was determined by measuring the case temperature of the package. If the difference between five consecutive case temperatures measured at every 1min interval is less than 0.1^0C, the package had reached thermal stability at its ambient. Then the reverse biased current-voltage (I-V) sweep is initiated from -10V – 0V. The forward biased I-V

sweep was initiated immediately after from 0V-3.7V. In order to minimize the impact of junction heating during I-V sweep, a pulse current with a 1ms pulse width and a 10% duty ratio was used.

The temperature characterization of I-V characteristics was performed by adjusting the cold plate temperature from 25^0C to 75^0C in 5^0C increments. The procedure mentioned in the above paragraph is repeated at each temperature condition. During the aging study periodic electrical characterizations were performed off-line. The same protocol as mentioned above is used with the cold plate temperature at 25^0C.

2.7 Results

Electrical parameters such as, series resistance, ideality factor, and reverse leakage current was extracted from the current-voltage characteristics curves, measured at different time intervals. There are two catastrophic failure modes observed during the study, open and short circuit failure. It was hypothesized that electromigration was the dominant failure mechanism, that causes these failure modes. The evidence that proves and disapproves this hypothesis is presented in this section.

2.7.1 Electrical parameter extraction

Extracted I-V data over the life time of the sample were analyzed to extract series resistance, ideality factor at the recombination current region, and ideality factor at the tunneling region. Figure 16 shows the three regions of interest.

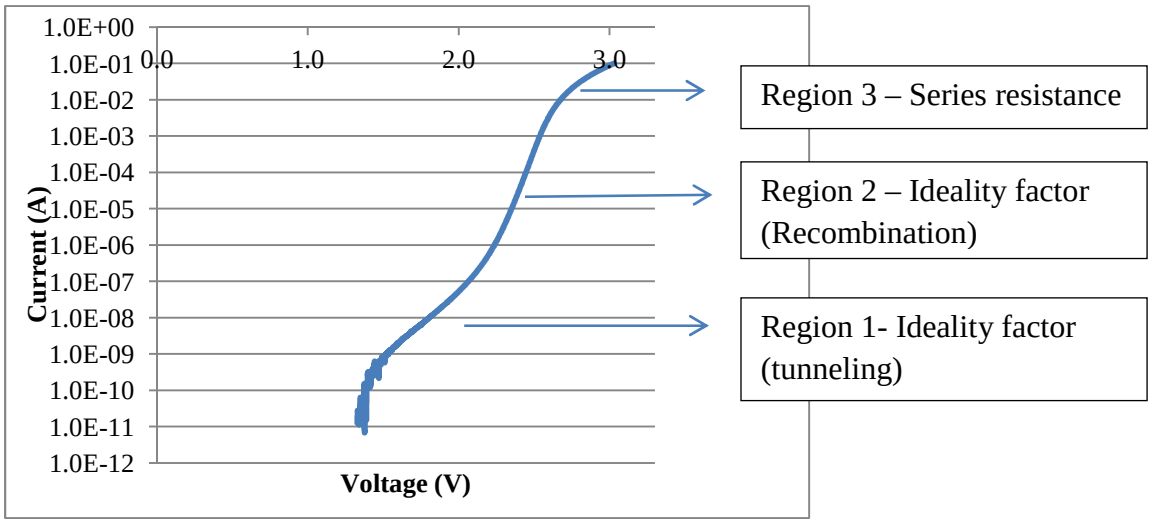


Figure 16. Current-voltage (I-V) curve with three regions of interest for data analysis

The diode conduction equation, for the electrical model discussed in section 2.2, can be written as,

$$I - \frac{(V - IR_S)}{R_p} = I_s\,(e^{q(V-IR_s)/(nkT)}\text{-}1). \qquad \text{equation D}$$

Where, I – forward current, I_s – saturation current, V- forward voltage, R_s – series resistance, R_p – parallel resistance, q – electron charge, k- Boltzman constant, T- temperature (K), and n – ideality factor.

For regions 1 and 2, the current is small; therefore, the effect of series resistance is negligible. Further the parallel resistance is large so its impact is also negligible. Therefore, the diode conduction equation can be simplified as,

$$I = I_s\,(e^{q(V/nkT)}\text{-}1). \qquad \text{equation E}$$

In region 3, the effect of series resistance is significant; therefore, following equation was used to extract series resistance.

$$I = I_s\,(e^{q(V-IR_s)/(nkT)}\text{-}1) \qquad \text{equation F}$$

The measured current-voltage data were fitted using equation E for, region 1 and 2. The two fitting parameters were equivalent to, I_s, and q/nkT. Two different ideality factors and saturation currents were extracted from regions 1 and 2. At region 1, space charge recombination, and tunneling currents dominate the electrical transport characteristics. In this region measured ideality factors are several times greater than 2. Instead of ideality factor, a more appropriate term would be tunneling coefficient, since tunneling currents dominate current transport.

The exponential fit of I-V data in region 2, for an LED package is given in Figure 17. The fitting parameters (a and b) along with their 95% confidence band limits are given in the inset. The ideality factor can be calculated using the following equation.

$$19.32 = \frac{q}{nkT}$$

Where, q=1.602e-19, k = 1.38e-23, and T = 298K

Therefore, for this case the ideality factor is 2. This is the region, where recombination currents are the dominant carrier transport mechanism for wide band gap semiconductors. Therefore, an ideality factor closer 2 is expected. There is a wide variation in ideality factor between samples (1.5-2.4).

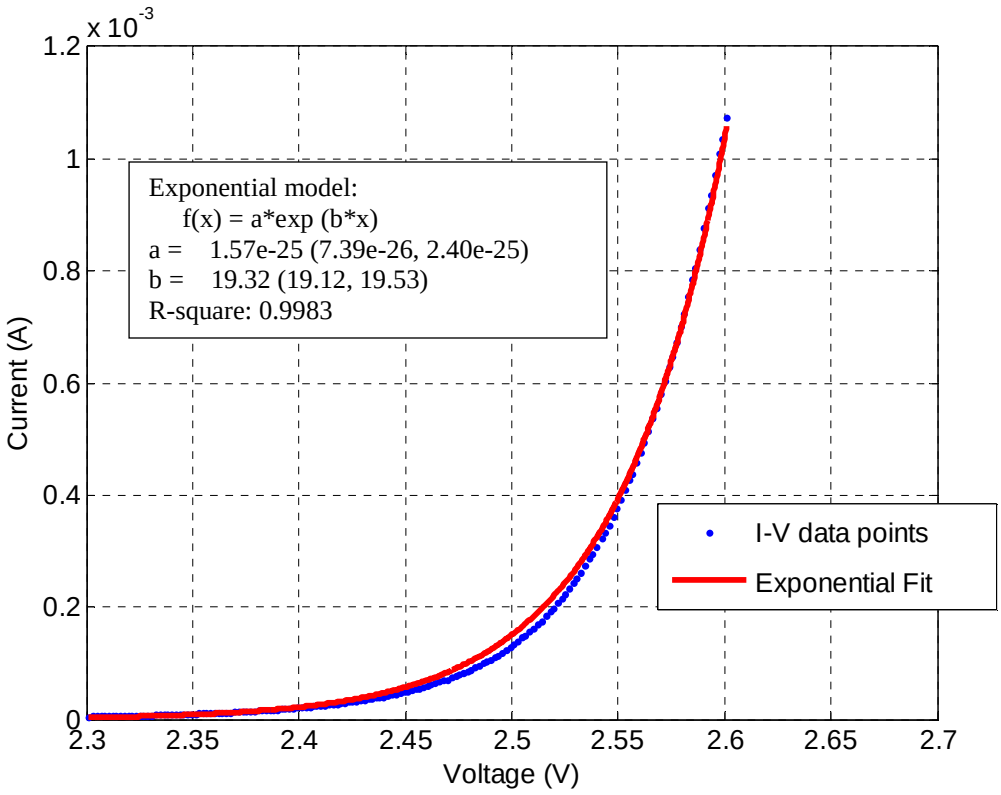


Figure 17. Exponential fit of current – voltage data for an LED package at recombination current dominated region

In order to extract series resistance from measured I-V data, the equation D was rearranged as follows,

$$V = \frac{nkT}{q} \ln\left[\frac{I}{I_s} \exp\left(\frac{qIR_s}{nkT}\right)\right].$$

The I_s, and n values are known from the exponential fit results from the recombination region. The current-voltage data for the region where series resistance is significant is plotted and the above relationship was used as the curve fitting model with R_s as the fitting parameter. The junction heating effect reduces the series resistance value. Therefore, for series resistance extraction, only measured data points for currents less than 100mA was considered. An example of an LED package, where the above mentioned theoretical model was fitted to an experimental data set is given in Figure 18. The extracted series resistance, with its 95% confidence band is indicated in the inset.

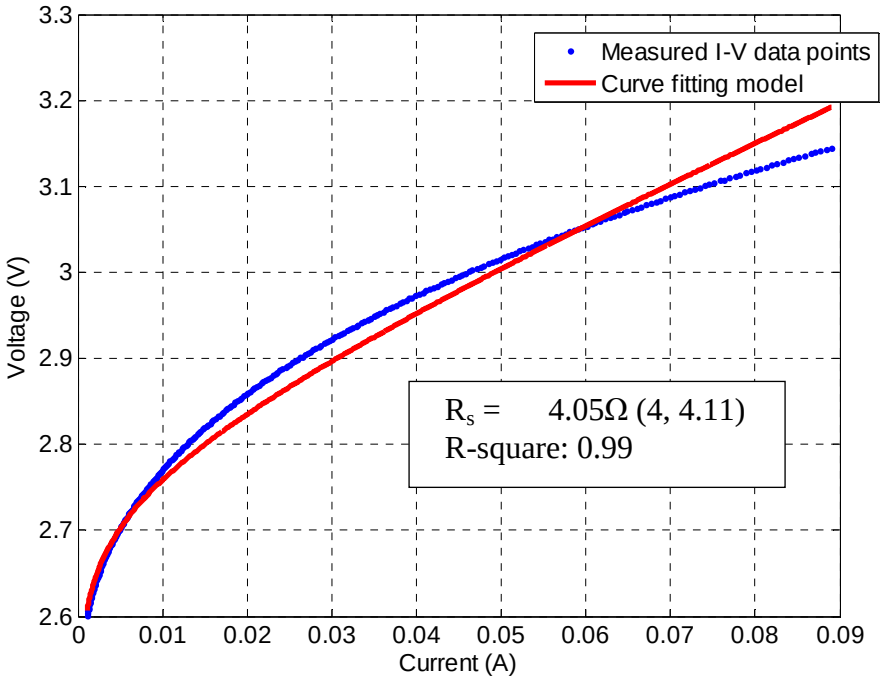


Figure 18. The measured I-V data and the data points calculated by the curve fitting model, with series resistance as the fitting parameter

2.7.2 Series resistance change with time

The extracted series resistance is normalized to the initial value. In certain stress conditions, there is a short-term reduction in the series resistance, at the start. This could be due to the annealing effects that improve the ohmic contact properties of the LED package [105]. The series resistance after annealing was considered as the initial resistance.

$$\text{Normalized Resistance} = \frac{\text{Measured Resistance } (\Omega)}{\text{Initial Resistance } (\Omega)}$$

The normalized series resistance change with time at different temperature stress conditions are plotted in Figure 19. The averages of five samples are plotted, except in the case of 448K condition, where meaningful data for only three samples were possible. The time axis is normalized to the time at which the last measurement point was measured prior to failure. The error bars include standard error of the mean within the group and measurement error. The measurement errors are significantly small when compared within the group deviations. The samples at 413K and 423K stress conditions showed short circuit failure, whereas, samples at 448K showed open circuit failure. The absolute data used for the normalization is provided in appendix B.

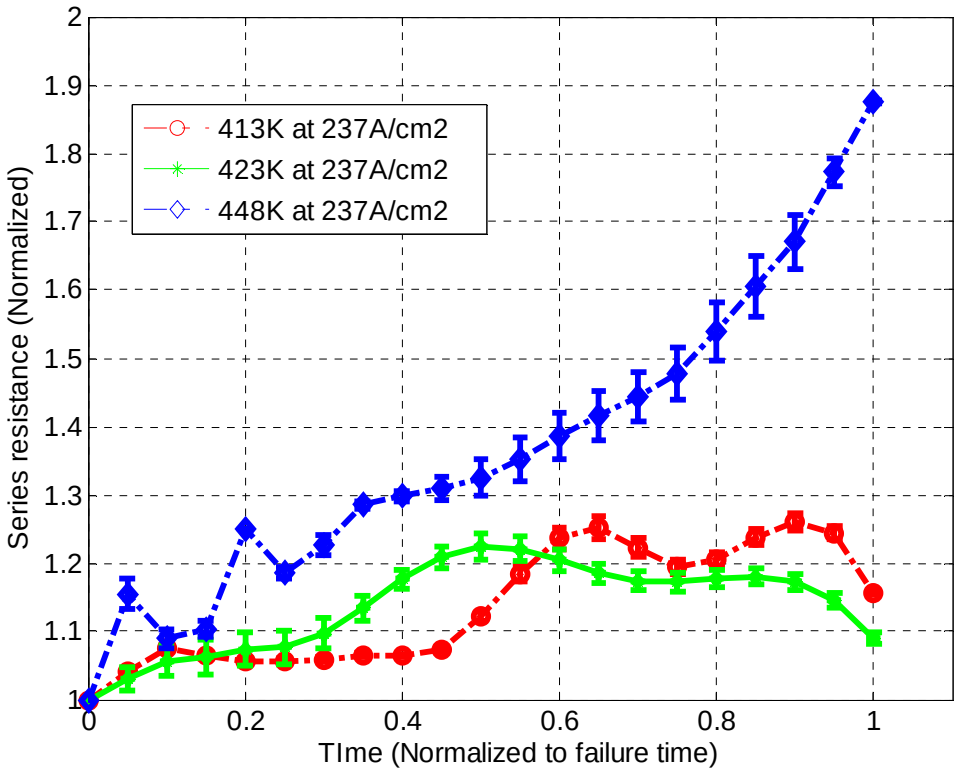


Figure 19. Series resistance change with time at three different junction temperatures

The normalized series resistance change with time, at different current densities is plotted in Figure 20. The data points represent an average of five samples. All samples, except a sample at 355A/cm^2 showed short circuit failure. The sample that showed open circuit failure was not included in the data for Figure 21.

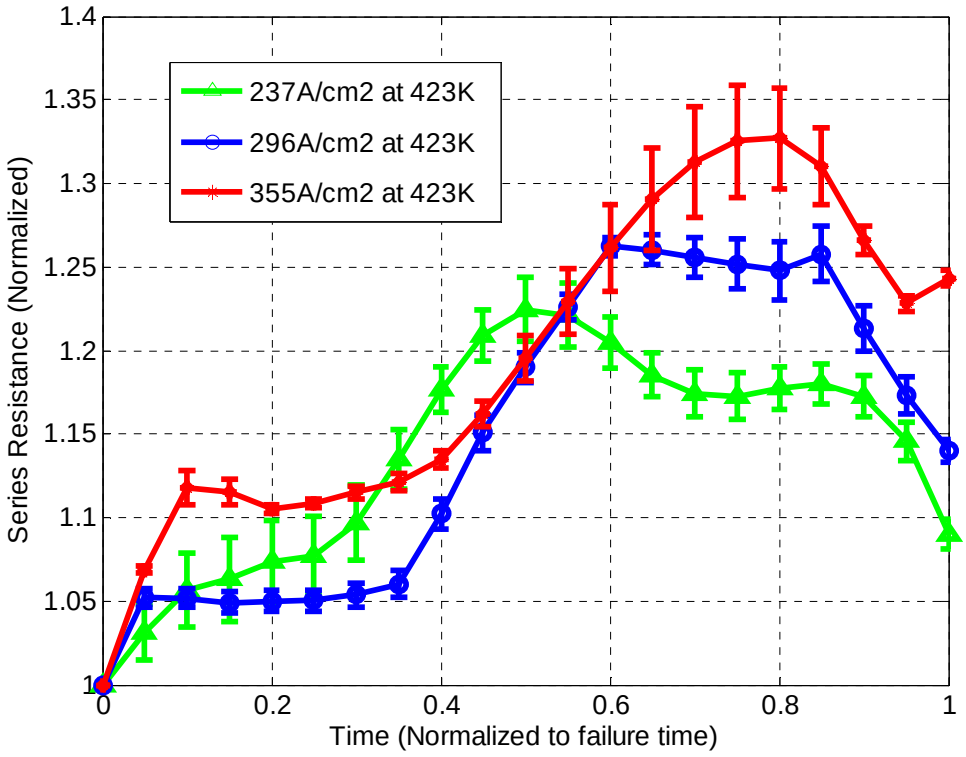


Figure 20. Series resistance change with time at different current densities

2.7.3 Failure mechanism: electromigration

As explained two types of catastrophic failure modes were observed during the study. They are, short circuit failure, and open circuit failure. A failure mechanism that could explain both types of failures is electromigration. The current flow and temperature in the contact metallization layers cause migration of metal atoms. These metal atoms create voids in the contact metal. The area surrounding the voids will have high current densities, which will further accelerate the electromigration process. The nucleation and growth of voids in metal conductors would lead to an open circuit failure.

The contact metallization layers of the LED sample is Au/Ni. There are no reported activation energies of electromigration of Au or Ni into GaN. If the reported activation energies for GaAs were used as the reference, then Au has a lower activation energy than Ni [48], [106], [107]. Which means Au is more likely to migrate into the semiconductor than Ni. The migration of Au occurs in the direction of electron flow. Therefore, voids are formed near the cathode [108], [109].

The migrated metal atoms would accumulate at the surface of the semiconductor. The GaN –buffer layers would have a high density of defects (10^{7}-10^{9} cm^{-3}) that was formed

during the material growth phase. These defects act as vacancies for metal atoms to migrate. This will lead to formation of metal spikes within the semiconductor. These metal spikes will grow into the active region with time and causes a junction short-circuit. This failure mechanism is illustrated in Figure 21. A study that looked into migration of impurities in AlGaN/GaN HEMTs reported activation energy of 0.26eV for impurity migration along dislocations[51]. However, they claimed higher thermal activation energy for device failure. This failure mechanism was also observed in GaAs-based devices [61], [63], [65], [66], [91], [92].

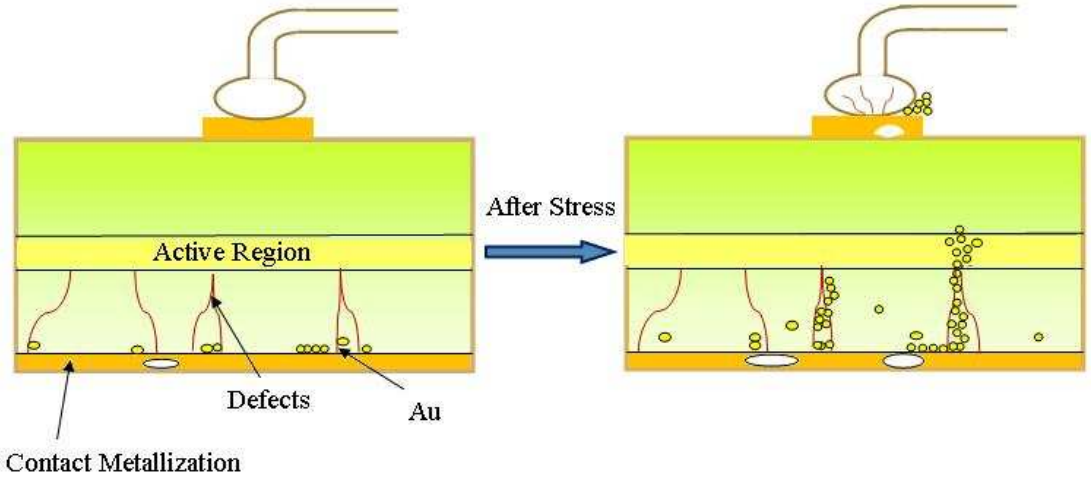


Figure 21. Illustration of formation of metal spikes due to electromigration

2.7.4 Analysis of series resistance change with time

There are four distinct phases that could be observed in series resistance variation with time. The four phases are marked in the Figure 22. The phase 1 is where there is a step increase in series resistance after which there is no significant change. Even though during this period void formation occurs it will not lead to a measurable change in series resistance. This latency period was also observed by studies that looked into electromigration in metal contacts in semiconductor packages [110], [111], [112], [113]. The latency period should be shorter for LED packages that were subjected to higher temperature or current stress. This is because the void growth is accelerated by these stress conditions. The experimental evidence at different stress conditions supports this claim.

The second-phase is where there is a monotonic increase in series resistance. In this region series resistance increase has a linear dependence with time. In this region, void is

already formed and the resistance of the metal is comprised of two series resistances [110], [111]. The equivalent resistance is,

$$R(t) = \frac{\rho_b L_b}{A_b} + \frac{\rho_c (L - L_b)}{A_c}.$$

Where, ρ – resistivity, L_b – length of the void, A – area, L- length of the conductor, b- barrier layer, and c - conductor

The resistance change rate can be found by taking the derivative with respect to time.

$$\frac{\partial R}{\partial t} = K \times \left(\frac{\rho_b}{A_b} - \frac{\rho_c}{A_c}\right) \times \frac{\partial L_b}{\partial t}$$

Where, R – normalized resistance, and K – constant

Based on the above equation it could be stated that the resistance change rate is proportional to void growth rate. During phase 2, this growth rate is constant for a given temperature and current. For a very long conductor with no back flow, the vacancy flow velocity induced by electron wind force can be written as [53],

$$V_{FM} = Bz^* e\rho j.$$

Where B – mobility, z^* - effective charge, e – electron charge, ρ – resistivity of material, and j-current density

The vacancy flow velocity is equal to void growth rate; therefore, resistance change rate at phase 2 can be expressed as below.

$$\frac{\partial R}{\partial t} = \frac{D_0 e^{-\left(\frac{Q}{kT}\right)}}{kT} z^* e\rho j \qquad \text{equation G}$$

Where, k – Boltzman constant, T – temperature, Q – activation energy, and all other terms have the same meaning as expressed above.

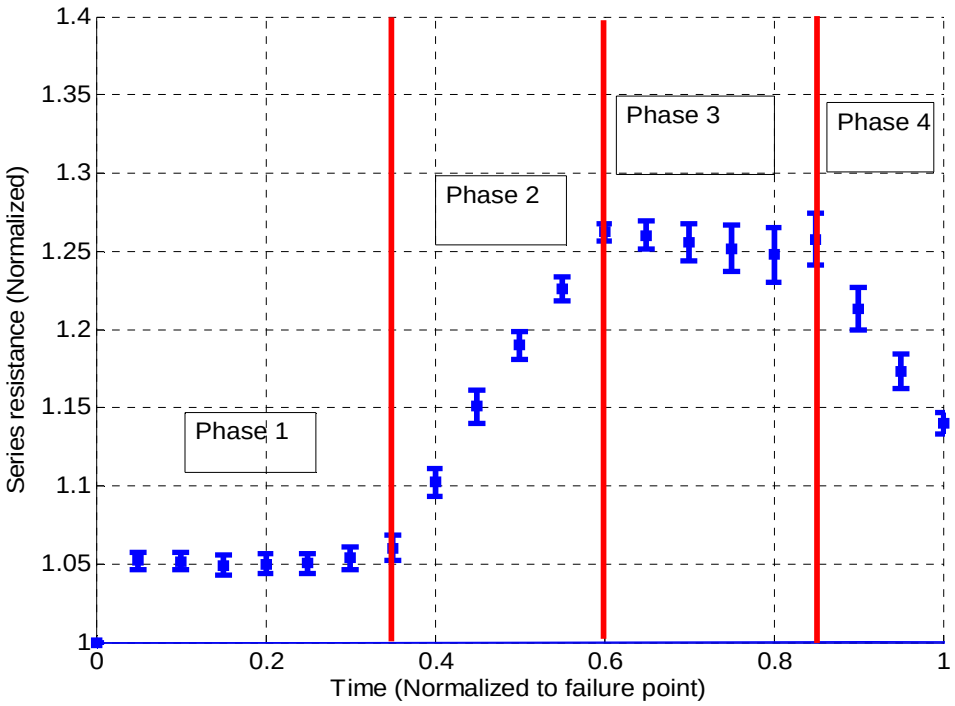


Figure 22. Series resistance change with time for an LED package at 423K and 296A/cm^2

At 448K temperature condition, shown in Figure 23, there is a linear increase in series resistance with time. However, there is a pivot point where there is a clear separation of slopes. That point separates the two phases for this condition. The physics of failure for the first half is same as the phase 2 failure explanation given above; therefore, it is referred to as phase 2. The failure mechanism for the other half is different; therefore, it is referred to as phase 5.

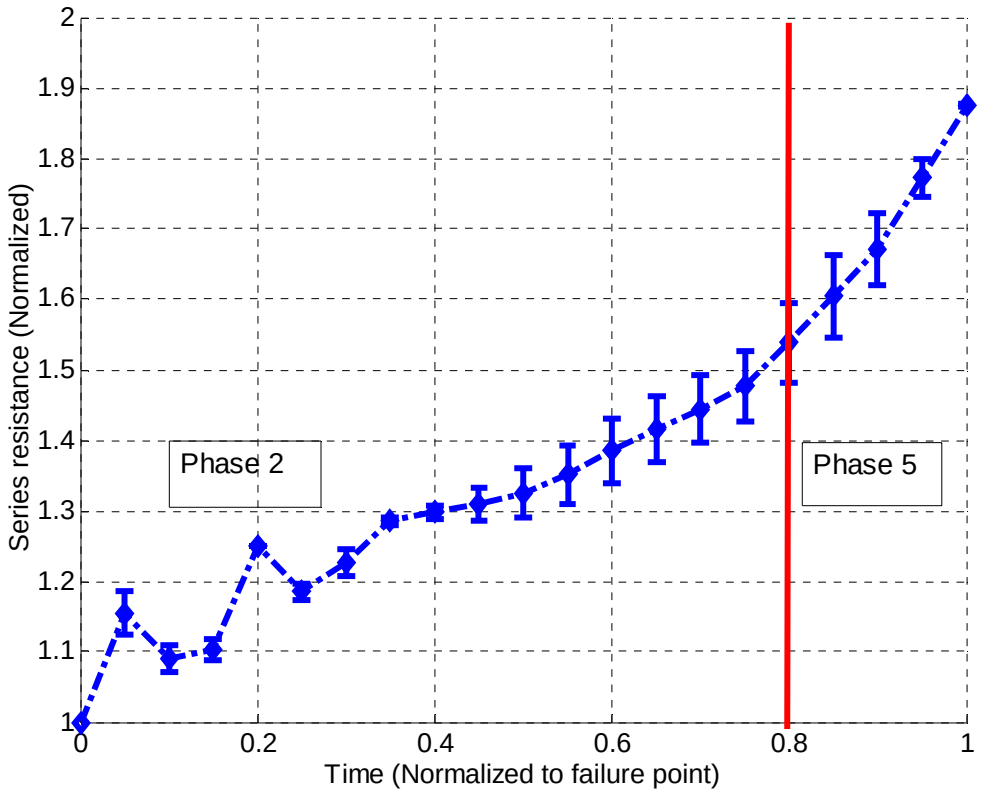


Figure 23. Series resistance change with time at 448K and 237A/cm^2 current density

Phase 2 slopes at different temperature conditions are given in Figure 24. The data points in the figure represent the average slope of samples at each condition. The error bar represents the standard deviation of slopes within the same group. Using equation G and Figure 24, the activation energy for vacancy diffusion can be extracted. The activation energy for vacancy diffusion is 0.47±0.09eV. The contact metallization layer in the LED package was a Ni/Au alloy. The reported activation energy for Au migration on GaAs substrate was 0.59±0.09eV [44]. The reported activation energy was extracted using the Blacks' mean time to failure model for electromigration. However, both the experimental value and reported value for Au vacancy migration are comparable.

The phase 2 slopes at different current densities are plotted in Figure 25. If one may go by the equation G, the resistance change rate is proportional to current density. However, the empirical model developed for resistance change in Cu conductors due to void growth indicates that [111],

$$\frac{\partial R}{\partial t} \propto j^n \ .$$

Where n- current exponent, and j-current density

This is a convenient relationship, because even Blacks' model has a current exponent. The physics based models that analyzed the void formation process in a conductor due to electromigration describe two mechanisms, void nucleation and void growth [50], [114], [115]. The void nucleation has current density squared (j^2) dependence, whereas void growth rate has a linear dependence with current density. The above empirical relationship along with Figure 25 was used to extract a current density exponent of 1.5±0.2. The current exponent show that resistance change rate at phase 2 is influenced by the void growth process.

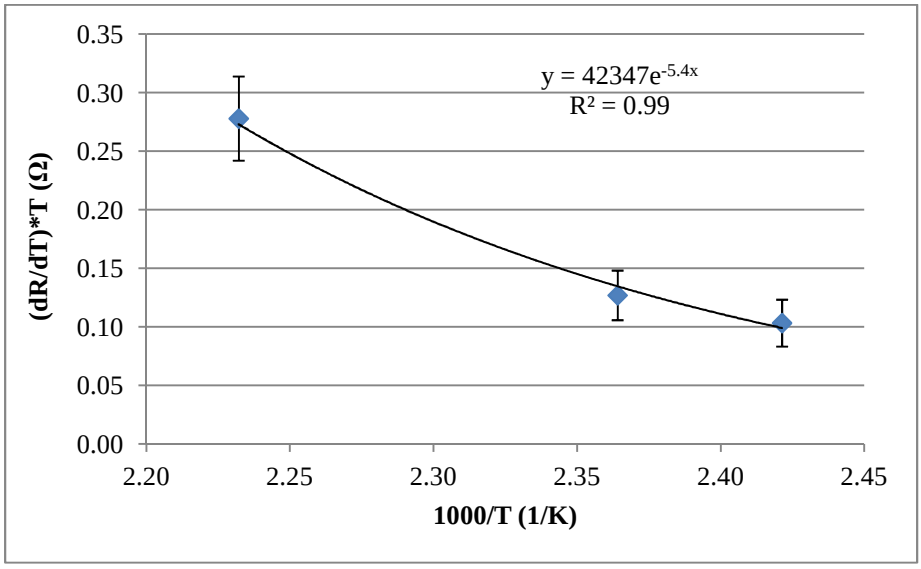


Figure 24. The series resistance slope variation with junction temperature

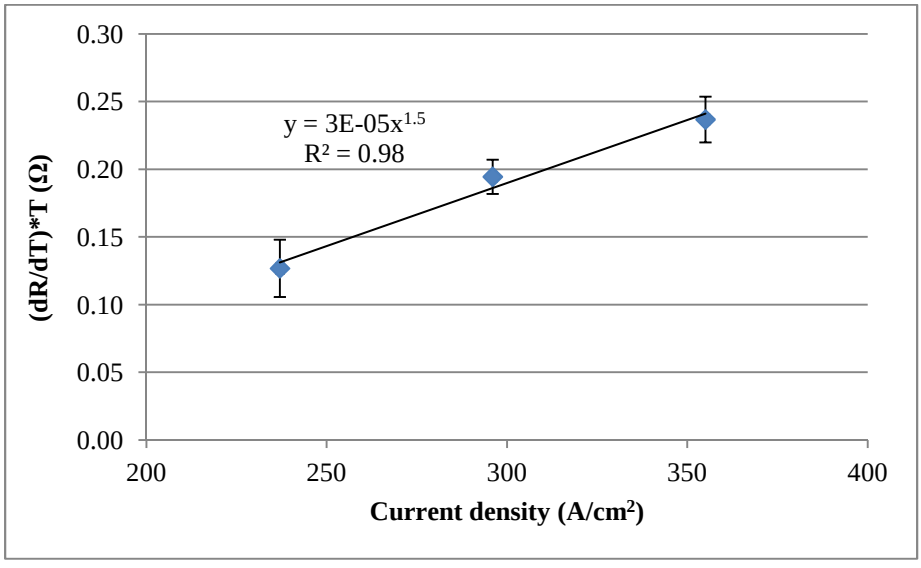


Figure 25. The series resistance slope variation with current density

The phase 3 in Figure 22 is the region where there is very little change in series resistance. The series resistance has a ±0.025 oscillation in this region. The drift velocity of ions or vacancies could be explained using the following equation proposed by Blech [53].

$$v = Bz^{*}e\rho j - B\frac{\Delta F}{l}$$

Where, B – mobility, z^{*} - effective charge, e – electron charge, ρ – resistivity, j-current density, ΔF – free energy difference between two ends of a conductor, and l –conductor length

The mass flow in the conductor creates a concentration and stress gradient within the conductor. These forces act in the opposite direction of the electron wind force; therefore, have a damping effect on flow of ions. This could not only diminish the void growth rate but could also heal some voids. Blechs' critical length theory says that if the length of the conductor is less than the Belch critical length, the voids completely heal due to back flow [53].

Phase 4 in Figure 22 is the onset of short circuit failure in the LED package. Electromigration facilitate the diffusion of metal impurities into the semiconductor. When metal spikes reach the active region of the die, short-circuit failure would occur. The growth of metal spikes into the active region would create low resistance current paths. Typically the active region of the device is in nm scale; therefore, when metals reach the boundary of the active region, metal concentration within the active region increases rapidly. The rapid decline in series resistance in phase 4 can be attributed to the rapid concentration growth of metals in the active region.

It was hypothesized that diffusion is the dominant transport mechanism of metal atoms that migrate into the active region. The Ficks' second law of diffusion can be used to express the concentration at a fixed location as a function of time.

$$C(x,t) = C(surface,o) \times (1 - \text{erf}\,(\frac{x}{\sqrt{Dt}}))$$

Where, x – distance from the surface, t – time, and D- diffusion coefficient

If the initial concentration of metal is assumed as a thin sheet of infinite concentration, located at an arbitrary position X_0, then the diffused concentration can be expressed as a Gaussian concentration profile.

$$C(x,t) = \frac{N}{\sqrt{\pi Dt}}e^{-\frac{(x-x_0)^2}{4Dt}}$$

Where, N- number of metal atoms per unit area, D – diffusion coefficient, t –time, and x – distance with respect to an arbitrary location

If assume that the surface with the infinite concentration of metal as the metallization layer next to the semiconductor, metal concentration at a fixed location over time can be stated as,

$$C(t) = At^{-\frac{1}{2}}\exp\left(-\frac{b}{t}\right). \qquad \text{equation H}$$

Where, b and A are temperature dependent constants.

It was shown in previous electromigration studies on Au contact metals that Au migrates from anode to cathode (in the direction of electron flow). Therefore, we can assume that Au migrate from P-contact layer. If the fixed location is closer to the n-type GaN layer, then increase in concentration in that location will contribute towards short circuit failure. It was assumed that series resistance change in phase 4 of Figure 22 is dominated by this concentration increase. Then it could be stated that the rate of increase of concentration is proportional to rate of decrease of series resistance in phase 4.

$$\frac{\partial C(t)}{\partial t} = -k \times \frac{\partial R(t)}{\partial t} \qquad \text{equation I}$$

Using equations H and I, series resistance just before failure could be expressed as below.

$$R(t) = A \times t^{\frac{-1}{2}} \times \exp\left(-\frac{b}{t}\right) + C$$

Where, $b = \frac{x^2}{4D}$, $A = \frac{N}{\sqrt{\pi D}}$, and C – constant

The above model was fitted to the experiment data as shown in Figure 26. The parameter b, depends on the diffusion coefficient and therefore on temperature. This parameter was extracted for two temperature conditions with short circuit failure. The parameter showed the expected decreasing trend with temperature. As expected the parameter didn’t show a statistically significant change at different current densities.

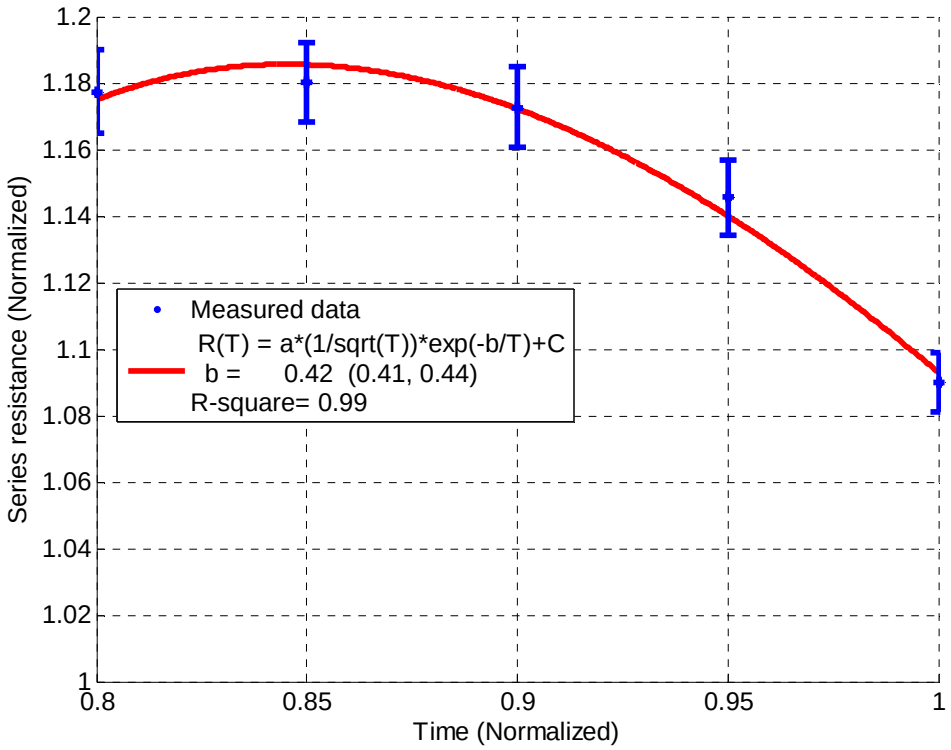


Figure 26. Variation of series resistance with time just before failure

2.7.5 Ideality factor change with time

The ideality factor of a diode is an empirical parameter that provides an indication of current transport properties in a P-N junction diode. The theoretical basis for ideality factor was established using the Shah-Noyce-Schokley theory, which was explained in section 2.2. The impurity migration and electrically active defects create traps closer to Fermi-level that act as recombination centers. It could be argued that an increase in impurities in the active region will lead to an increase in recombination current. The increase in recombination current in the LED leads to higher ideality factors.

The extracted ideality factor in this study as explained in section 2.7.1, showed an increasing trend with time. The ideality factor change at different junction temperature conditions as a function of stress time is presented in Figure 27. The ideality factor increase with time supports the hypothesis that migration of metal atoms into the active region is the failure mechanism that causes short circuit failure of the LED package. The ideality factor increase at the point of failure is smaller for LED packages that were operating at 448K junction temperature condition. These devices showed open circuit failure as opposed to short circuit failure observed in other stress conditions. This is plausible since formation of metal spikes into the active region is not associated with

open circuit failure. This also suggests, while metal migration along defect lines occurred in samples at 448K, there wasn't an adequate concentration of metals in the active region to cause short circuit failure. Some other failure mechanism intervened and caused open circuit failure in the LED package.

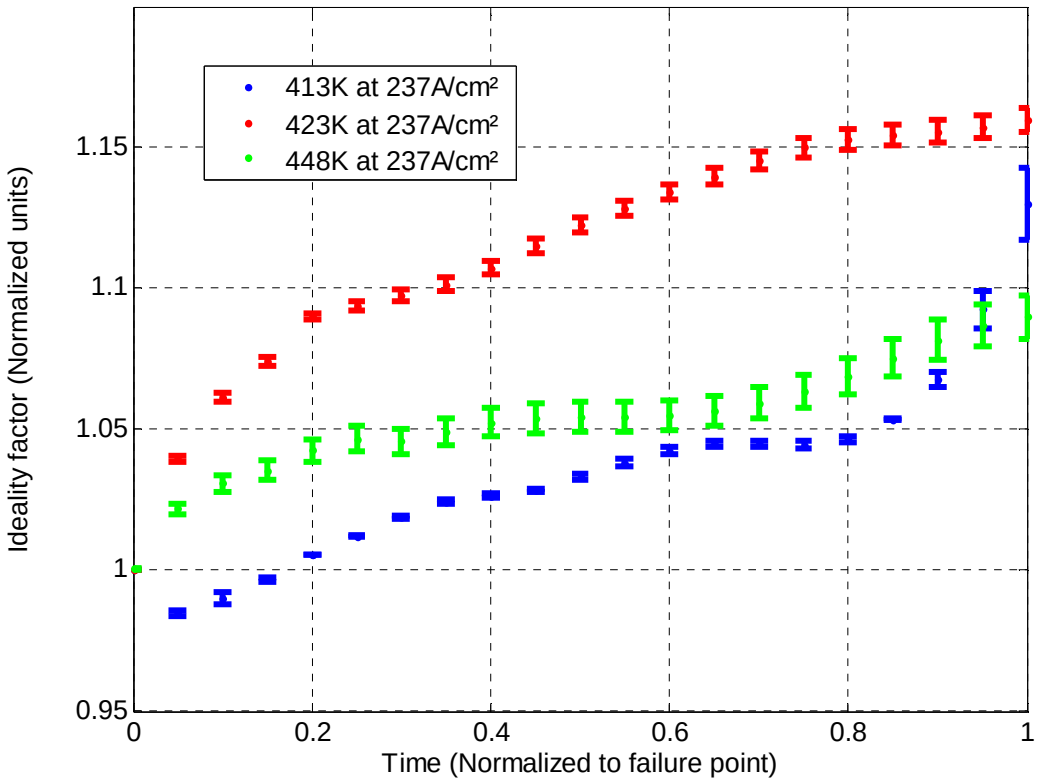


Figure 27. Ideality factor change with time at different junction temperatures

2.7.6 Reverse leakage current

An ideal diode will conduct only in the forward direction unless within permissible operating conditions. However, a real diode would have a current flow when reverse biased due to the presence of structural defects, impurities that form alternative current paths, and imperfect passivation layers. Current transport mechanisms such as tunneling, space charge recombination, and field enhanced thermionic emission are responsible for reverse leakage currents in GaN based LEDs [116], [117], [118]. The reverse leakage current and the associated mechanism, commands significant interest from the GaN based LED fabrication community. This is because of its ability to capture both bulk leakage current due to threading dislocations and surface leakage effects.

Past studies on GaN LEDs have shown that there is an exponential growth in reverse leakage currents with the threading dislocation density [118], [119]. The threading

dislocations form alternative current conduction paths into the die that facilitate carrier transport even to quantum well region. Reverse biased luminescence were observed in these devices due to recombination of carriers in the quantum wells [118]. However, areas of luminescence have a spontaneous spread, rather than a uniform distribution, supporting the hypothesis that there are dislocation paths in the die preferred by the current when reverse biased. Another hypothesis for large leakage currents in LEDs is defects in the passivation layer that leaves dangling bonds to facilitate surface currents [120]. These defects typically occur during the fabrication and not during aging.

The metal migration along defects was also hypothesized as a cause of increase in reverse leakage current [121]. In this study on flip-chip packages, authors observed AgS_x formation at the Ni/Ag contact. The AgS_x formed due electrolytic migration, has penetrated through the passivation to form a low resistance alternative current path. This leads to a significant increase in reverse leakage current with aging.

When metal spikes form due to electromigration in Ni/Au metallization layer, those metal atoms could migrate into dislocations. The dislocations with metals atoms form low resistance alternative current paths in the device. The metal migrations initiate in the buffer regions and then expand into the active region of the LED. The reverse biased current flows through these dislocations infused with metal atoms. Therefore, increase in reverse leakage currents in the LED is another indicator of metal migration. This is evident in Figure 28, where variation of reverse leakage current with aging from an LED package operating at 423K junction temperature and 237A/cm^2 current density is given.

Figure 29 shows the variation of measured reverse leakage current at -10V with time, for four different LED samples at different stress conditions. There were two samples that showed the short circuit failure mode and another two samples that showed open circuit failure mode in this figure. The samples that showed short circuit failure mode has a larger increase in reverse leakage current than the ones with the open circuit failure mode. This further proves the fact that in the case of short circuit failure, large scale migration of metals into the semiconductor occurs.

It could be argued that reverse leakage current increase is associated with the increase in defect density with aging. The dislocations in the die could expand with aging leading to an increase in reverse leakage currents. The expansions of dislocations further facilitate metal migration as dislocation offers a lower barrier path for metals to migrate. The stresses created in the lattice due to dislocation aid the transport of metal through the lattice in the active region [51]. Further, dislocations don't cause catastrophic failure in a GaN device, unless they become electrically active and grow exponentially with time. However, generation and movement of dislocations can facilitate catastrophic failure by acting as a low barrier path for metal diffusion into the semiconductor.

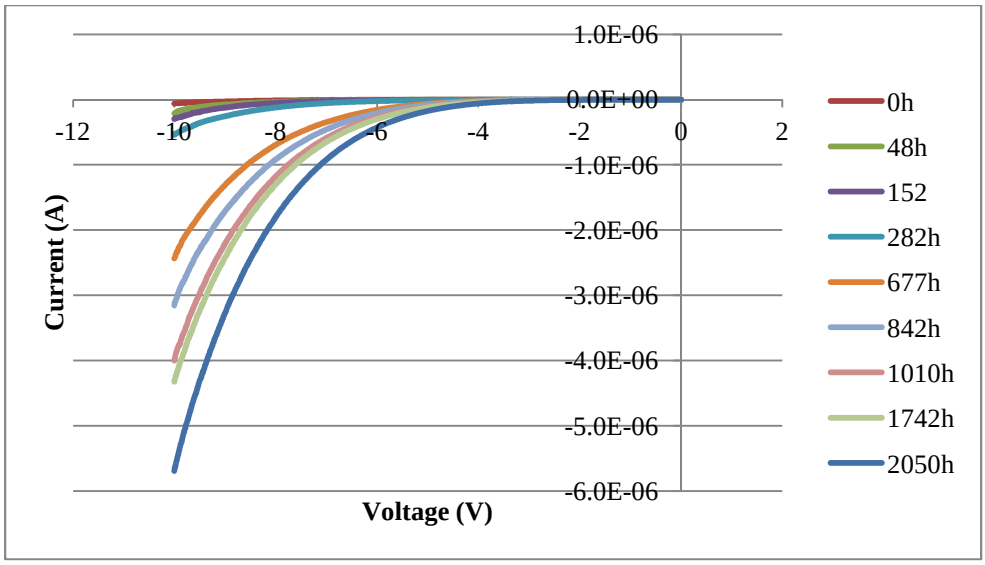


Figure 28. Reverse leakage current increase for an LED package at 423K junction temperature, and operating at 237A/cm^2

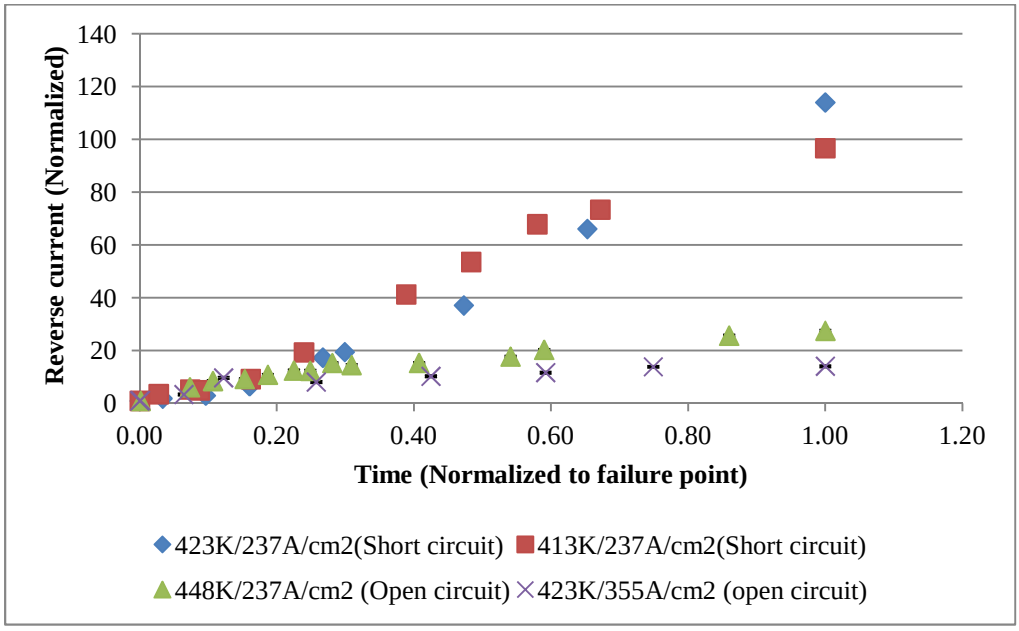


Figure 29. Reverse current change for LED packages at different stress conditions

2.7.7 Blacks' model

Black developed a model to estimate the median time to failure (MTF) of a conductor due to electromigration when subjected to current and temperature stress conditions [41].

$$MTF = \frac{KATexp(\frac{Q}{kT})}{J^n D_o}$$

Where, K – proportionality constant, A- cross sectional area of the metal film, T – temperature, J-current density, Q- activation energy, k – Boltzman constant, D_0 – pre-exponential factor, and n-current exponent

Black showed that n=1, if the electromigration depend on the structural variations of the conductor, and n=2, if temperature gradient within the metallization layer is the cause of electromigration.

The empirical model used by the semiconductor industry to determine electromigration life of a conductor is a modified version of the above mentioned Blacks' equation [122].

$$MTF = K^* J^{-n} \exp\left(\frac{Q}{kT}\right)$$

Where, K^* is a constant that depends on material properties and geometry.

The median time to failure in this experiment is defined as the end of phase 2 as defined in Figure 24 and Figure 25. As explained in previous sections the actual failure occurs due to growth of metal spikes that short the junction. Electromigration enable this process through mass transport to semiconductor layer. Up to phase 2 resistance change is dominated by void growth initiated by electromigration. At constant current density condition above, equation is reduced to the Arrhenius relationship.

$$MTF = K_1 \exp\left(\frac{Q}{kT}\right)$$

At constant temperature the above equation is reduced to,

$$MTF = K_2 J^{-n}.$$

These two relationships are plotted in Figure 30. The activation energy for electromigration is 0.46±0.06eV. This is very similar to the activation energy measured in 2.7.4, using resistance slope. This is expected since both approaches measured the activation energy of the vacancy diffusion. The reported activation energies for self-diffusion of Au in Au contacts range from 0.4-0.9eV. The wide variation in reported activation energy values were attributed to different substrate materials, stress conditions, and measurement methods. There is no known study that measured activation energy of an Au contact on GaN substrate. The activation energy of Au migration in contacts on

GaAs substrate is 0.59±0.09eV. The activation energy is lower for GaN substrates. This may be due to higher defect density in GaN layer that facilitate vacancy diffusion in Au. However, there is no statistical difference between the activation energy measured in the experiment for Au on GaN and activation energy reported for Au on GaAs.

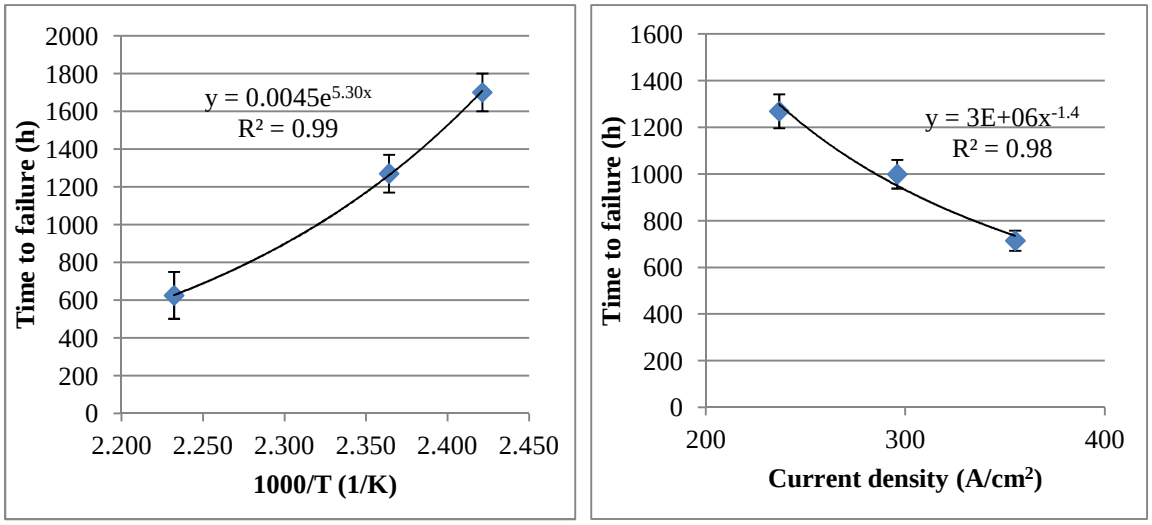


Figure 30. Mean time to failure with temperature (left) and mean time to failure with current density

The measured current exponent is 1.4±0.2. This is very similar to the current exponent measured in 2.7.4 using resistance slopes. Even though current exponents between 1 and 3 have been observed in experiments, there is no theoretical basis to explain the fractional values of n. It could be theoretically established that n is equal to two, when void nucleation occur due to electromigration [115], [123]. Electromigration also depend on drift velocity which is inversely proportional to current; therefore n is equal to one [41]. It was hypothesized that electromigration has two phases, void nucleation and void growth [115]. The duration of each phase with respect to total failure time will determine the current exponent. The measured current exponent suggests that void growth phase dominates the failure time defined in the analysis. A discussion on recent improvements to the electromigration life time models and implication of those models on reported activation energies and current exponents are provided in appendix C.

2.8 Chapter summary

A systematic study on series resistance change of an InGaN LED package at different current and temperature stress conditions are presented. The series resistance of an LED package is an indicator of the health of its electrical contacts. Therefore, by analyzing the variation of series resistance over time, the degradation and eventual catastrophic failure of electrical contacts is established. Long term degradation studies on GaN- based LED packages in past literature observed that series resistance increase with aging. These studies hypothesized that this series resistance increase was due to degradation of ohmic contacts. However, none of these studies developed a relationship between series resistance change of the LED package to stress conditions or time to failure. This knowledge is essential to develop a failure prediction model based on series resistance.

This study investigated the series resistance change at different temperature and current stress conditions. This was designed as a two part study, where one part of the study kept junction temperature constant while changing the current, and the other part kept constant current while changing junction temperature. The key findings of the study are summarized below.

- Two catastrophic failure mechanisms, open circuit and short circuit failure were observed. In the case of short circuit failure, metal spiking into active region was identified as the failure mechanism. Electromigration facilitated the movement of metal atoms from the metallization layers to semiconductor surface.
- There are four distinct phases that series resistance goes through before failure. Phase 1 – latency period with little or no change in series resistance, phase 2 – series resistance increase with time, phase 3 – saturation period, and phase 4 – failure region.
- The series resistance increase rate at phase 2 depends on junction temperature and current density. Relationship between series resistance change rate and stress conditions were developed using the theory of electromigration.

  $$\frac{\partial R}{\partial t} = \frac{D_0 e^{-(\frac{Q}{kT})}}{kT} z^* e \rho j^n$$

  Where, k – Boltzman constant, T – temperature, Q – activation energy, ρ – resistivity, e – electron charge, D_0 – pre-exponential factor, n-current exponent, and z^* - effective charge
- Activation energy of 0.47±0.09eV and a current exponent of 1.5±0.2 were extracted from the series resistance rate change data at different stress conditions. This is comparable to values calculated from Blacks' model and reported values for self-diffusion of Au in an Au metallization layer on GaAs substrate.
- Series resistance just before short circuit failure is dominated by diffusion of metals into active region. A model was developed using Ficks' second law of

diffusion to define normalized resistance at time, t. Au migration occurs in the direction of the electron flow. It was assumed that series resistance decreases with time, when metal concentration at a fixed location closer to n-GaN layer increases.

$$R(t) = A \times t^{\frac{-1}{2}} \times \exp\left(-\frac{b}{t}\right) + C$$

Where, $= \frac{x^2}{4D}$, t- time, x- distance from the p-contact, and C – constant depends on initial condition.

- The model showed a good fit to the experimental data. This knowledge is useful in developing a pattern recognition algorithm to capture short circuit failure.
- The experimental data showed a good agreement with Blacks' model. The Blacks' model is useful in obtaining a-priori estimate of electromigration life of an electrical contact when the model parameters are known.
- Blacks' model parameters estimated using failure time data and series resistance change rate data (at phase 2) shows good agreement. This is very useful in reducing the testing time required to estimate model parameters.
- Reverse leakage current and ideality factor increased with aging. The behavior of these parameters suggests that diffusion of conductive impurities into active region occur with aging. High defect density in GaN facilitates this process.
- In the case of open circuit failure, the evidence suggests another failure mechanism intervened and accelerated its failure; before, electromigration induced metal atoms migrate into active region at sufficient concentration.

3 Thermal parameter study

In chapter 2 an electrical parameter, namely, series resistance that can signal failure of an LED package during operation was studied in detail. Not all failure in an LED package can be detected using electrical parameters because the electrical and thermal paths may or may not overlap. There are catastrophic failures that can result as a consequence of thermal path breakdown. Therefore, the objective of this chapter is to identify a thermal parameter that can augment the electrical parameter to make a comprehensive failure prediction strategy.

The junction temperature (T_j) of an LED package affects its light output, color, and reliability [27], [98], [124]. The heat at the junction is generated primarily due to non-radiative recombination of electrons and holes. The electrical input power to an LED package is converted to optical power and heat. Even with great advances that have been made in terms of efficacies of LED packages, on average 70% of the input power is converted to heat. Therefore, an efficient heat dissipation path is required to conduct heat generated in the junction to ambient.

The substrate material, submount, die-attach layer, thermal interface materials and heat sinks are critical elements in the thermal path that contribute to efficient heat transfer from the die to the heat sink. There is ongoing research and innovations in developing new thermal interface materials, substrates, package design methods, and bonding techniques to improve thermal conductivity between the die and heat sink. However, thermal expansion coefficient (CTE) mismatch, Young's modules mismatch, fabrication difficulties, and electrical insulation requirements have posed challenges to these efforts.

The degradation of thermal conduction path, due to delamination, voids and cracks would lead to an increase in operating junction temperature of the device. This can cause parametric failure, and catastrophic failure. The material layer that is subjected to the highest thermo-mechanical stress during operation is the interface material that bond two material layers. This is because of the shear stresses on the interface layer due to thermal expansion coefficient (CTE) mismatch.

Thermal resistance is a good qualitative indicator of the health of the thermal conduction path. Thermal resistance is a metric that is being widely used in the industry to estimate junction temperature of a device under a given environment and operating condition. Thermal resistance can be defined as, “the difference in temperature between two closed isothermal surfaces divided by the total heat flow between them [125].” It is essential that all thermal flux that crosses one isothermal surface crosses the other surface, without any heat generation or accumulation within the closed volume.

3.1 Literature review

In LED package design there can be an overlap between the current and thermal paths. The amount of overlap depends on the LED package design. For example, in the vertical package design shown in, there is separation of thermal and electrical path after the carrier substrate (submount). In flip-chip packages this separation happens even after the substrate. Failure mechanisms such as, electromigration induced void formation in metallization layers, and solder joint fatigue failures, that are discussed in sections 2.3.1 and 2.3.4, increase thermal resistance. A detailed discussion on thermal resistance measurement techniques are provided in appendix D.

3.1.1 Degradation of thermal interface

The studies that have analyzed thermal behavior of LED packages can be broadly categorized into two. The first category is the finite element analysis (FEA) studies to understand the change of thermal transport properties under specific stress or defect conditions [126], [127], [128], [81]. The other category is the experimental aging studies that subjected LEDs to specific stress conditions and monitored change of thermal parameters with aging [98], [99], [103], [129], [130], [131], [132], [133].

The semiconductor die, is attached to the substrate using a die-attach solder. This die-attach layer is the primary thermal interface in the package. Many past studies have cited delamination between different material layers, especially in the die-attach layer as the dominant failure mechanism that affect thermal resistance [22], [98], [103], [126], [128], [129], [131], [133]. The thermo-mechanical and hygro-mechanical stresses were identified as the primary causes of failure. The delamination at the die-attach layers in electronic packages leads to hot-spot formation triggering catastrophic failure [127], [134], [135].

Simulation studies showed that thermal and hygro-mechanical stresses cause delamination and voids in the die-attach layer between the chip and the substrate. This would lead to a significant increase in junction temperature [126], [128], [136]. Figure 31, below shows the increase in temperature of the Si layer of a MOSFET with the increase in the voided area percentage of the die-attach.

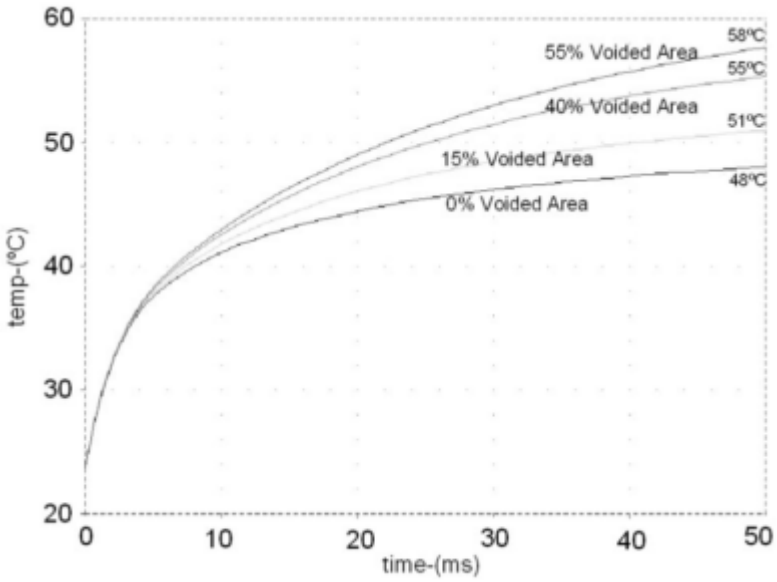


Figure 31. Predicted temperature vs. time curves for MOSFETs with voided area percentages [127]

Experimental long-term aging studies that measured thermal resistance over time showed conflicting evidence. One study measured a reduction in thermal resistance with time, whereas other studies reported an increase in thermal resistance. A study that subjected a flip-chip LED package to an ambient temperature of 85^0C and to a current of 350mA for 4000h saw an initial reduction, and a subsequent increase in thermal resistance as shown in Figure 32 [98]. A reliability study on flip-chip package reported a 5K/W increase in junction-to-case thermal resistance after 50h of operation at 400mA [102]. The estimated junction temperature at this current was 140^0C. The transient thermal analysis on the package showed that the degradation occurred at the die-attach layer between submount and substrate. A study that used 5mm indicator type InGaN and InAlGaP LED packages showed that the thermal resistance increase by 15K/W. The applied current stresses were 20, 40, 80mA at 25^0C ambient temperature [107].

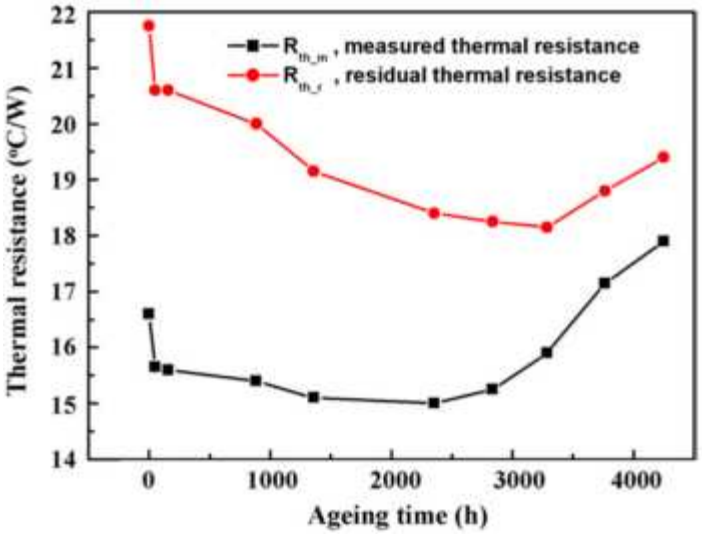


Figure 32. Variation of thermal resistance with aging time for an LED package [98]

3.1.2 Stresses on the thermal interface

LED packages are used in high temperature, humid environments. In these applications LED packages are subjected to both cyclical and stable temperature and humidity conditions. These lead to hygro-mechanical and thermo-mechanical stresses in LED packages [98], [126], [129], [133], [137]. Thermo-mechanical stresses are caused due to CTE and elastic modulus mismatch between different material layers.

The polymeric materials in LED packages (epoxy, die-attach solder, encapsulant, lens) absorbs moisture. The coefficient of moisture absorption is a material property. The differences in coefficient of moisture expansion (CME) of different materials cause hygro-mechanical stresses inside the package. At elevated temperatures hygro-mechanical stresses increase the thermal resistance [138], [128].

In modern LED packages thermo-mechanical stress due to CTE mismatch of materials is the primary stress factor that contributes towards delamination [128]. CTE mismatch induced thermo-mechanical stresses could occur at several key points in a package. The CTE mismatch between wire-bond and encapsulant would induce a strain on the wire-bond, weakening its bonding strength overtime. If the strain exceeds the bonding strength wire-bond lift-off occurs [71]. However, these studies used epoxy based encapsulant that have high CTE mismatch with Au and high Young's' modulus. However, use of Silicone as encapsulant and improvements in wire-bonding methods has reduced the significance of this failure mode. The lens on top of the encapsulant material is subjected to thermo-mechanical and hygro-mechanical stresses. This leads to development of fine cracks on

the lens that scatters light. The stress distribution and therefore, the possibility of developing cracks depend on the lens shape [139].

The thermo-mechanical fatigue would lead to creep, material fatigue and oxidization at the die-attach layer [81], [126], [127], [128], [131], [132], [133], [134], [137], [140]. All three of these mechanisms would degrade the material and induce deformations. If the deformations are irreversible, the material undergoes plastic deformation. One such plastic deformation mechanisms that materials undergo when subjected to prolonged stresses at high temperatures is creep. The Dorn-Weerteman power law states that [141],

$$\acute{\varepsilon} = \mathrm{A}\sigma^{n} e^{-(\frac{Q}{RT})}. \qquad \text{equation J}$$

where, έ – creep strain rate, σ – stress, n – stress exponent, q-activation energy, R – universal gas constant, and T – temperature

A further discussion on creep is given in appendix E.

3.1.3 Literature review summary

The die-attach layer is the primary thermal interface layer in an LED package. FEA studies and experimental studies show that thermal resistance of the LED package increase with delamination and void formation in the die-attach layer [127], [98], [99], [102]. In high power LED packages the thermo-mechanical stress play a dominant role in degrading thermal interfaces [103], [126], [137]. Stresses combined with temperature, applied over a period of time causes deformation in the thermal interface, which leads to delamination. The most probable form of deformation is the creep induced plastic deformation.

There are deformation models that correlate creep strain rate to stress and temperature. However, there is no study that investigated the possibility of developing a relationship between thermal resistance change rate, stress, temperature, and time to failure for LED packages. This knowledge is necessary to develop a failure prediction model that uses thermal resistance as the sense parameter.

3.2 Hypotheses

The objective of the study is to investigate the systematic change in thermal resistance of an LED package when subjected to different current and temperature stress conditions up to the point of catastrophic failure. The following hypotheses were formulated based on the evidence available in literature.

If an InGaN based LED package is subjected to thermal stress, by increasing the junction temperature, then the rate of change of thermal resistance irreversibly increases.

There is no evidence that links the thermal resistance change rate of an LED package with junction temperature. However, in the literature review section 3.1, it was established that creep strain is responsible for delamination and void formation in thermal interfaces. The creep strain rate increases with temperature. Therefore, it is plausible to hypothesize that the thermal resistance change rate depends on the junction temperature.

If an InGaN based LED package is subjected to current stress, by increasing the current density, then the rate of change of thermal resistance increases.

At high current densities, the temperature gradient experienced by different material layers in the package also increases. The high temperature gradients would increase the thermo-mechanical stress on the die-attach layer, due to CTE mismatch. The high stress would lead to high creep strain rate. Therefore, thermal resistance change rate would increase due to high current stresses.

In the context of above hypotheses, the following terms would have the following meanings.

- LED package refers to a single-die LED package. The definition of LED package is provided in section 1.1.
- Junction temperature refers to junction temperatures from 140^0C to 175^0C.
- Current density refers to current densities from 236A/cm^2 to 355A/cm^2. Current density is calculated as, operating current over die area. The above current densities correspond to operating currents from 1A-1.5A.
- Thermal resistance is defined as,

  $$R_{\theta J-C} = \frac{(T_j - T_{case})}{P_e}.$$

  Where, T_j – junction temperature, T_{case} - case temperature, and P_e – electrical input power. The case temperature is measured at the substrate.

3.3 Experiment design

The experiment was implemented in two parts. The first part is where the impact of junction temperature on thermal resistance change is investigated. The independent, dependent, and extraneous variables for this study are defined below.

Independent variables

- Junction temperature – The junction temperature (T_j) measurement procedure is explained in section 3.3.1. The T_j of the device was controlled by varying the case temperature. The three T_j conditions of 140^0C, 150^0C, and 175^0C were used.
- Stress time

Dependent variable

- Thermal resistance – The thermal resistance measurement procedure is explained in section 3.3.1.

Extraneous variables

- The operating current – the operating current was kept constant at 1A using a constant current LED driver.
- LED packages are mounted in same orientation
- The thermal resistance was measured at identical conditions. The ambient temperature was controlled at 25^0C and the applied current was 1A. The changes in the ambient temperature or heating current would change the thermal flux network and therefore, change the thermal resistance [125].
- Humidity – The humidity of the ambient air surrounding the package was not controlled during the study. Further, many of the materials used in LED packages have a low coefficient of water absorption. Therefore, it is anticipated that humidity would not have a significant impact on failure.

The second part of the experiment is to investigate the impact of current density on thermal resistance change. The independent, dependent, and extraneous variables for this study are defined below.

Independent variables

- Current –The drive current was controlled using a constant current LED driver. The currents used for this study are 1A, 1.25A, and 1.5A.
- Stress time

Dependent variable

- Thermal resistance – The thermal resistance measurement procedure is explained in section 3.3.1.

Extraneous variables

- The junction temperature – the junction temperature was kept constant at 150 $\pm 2^0$C by controlling the case temperature, using active and passive cooling.
- The thermal resistance was measured at identical conditions. The ambient temperature was controlled at 25^0C, LED packages were mounted in the same orientation, and the applied current was 1A. The changes in any one of these parameters would change the thermal flux network and therefore, change the thermal resistance [125].
- Humidity – The humidity of the ambient air surrounding the package was not controlled during the study.

The identical LED package described in section 2.6.1 was used for this experiment. The same set-up described in 2.6.2 was used for aging purposes. The thermal characterization was performed for all samples prior to testing, at three ambient temperature conditions (25^0C, 50^0C, and 75^0C). The cold plate temperature of the thermo-electric cooler is defined as the ambient in this study. Thermal resistance was measured periodically at 1A heating current and 25^0C ambient temperature. The measurement current is applied at 25^0C ambient temperature, and voltage is recorded before, applying the heating current. This measurement helps to avoid using the intercept of the calibration curve shown in Figure 34, in the calculations. The intercept is susceptible to large variations in response to marginal changes in the measurement environment. The gradient of the calibration curve depends on material properties, which remain stable during aging.

3.3.1 Thermal characterization

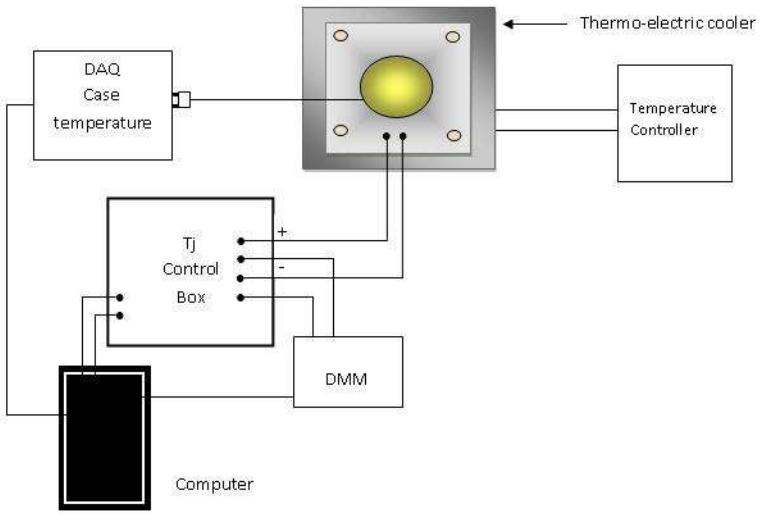


Figure 33. Schematic of the thermal characterization set up

Thermal characterization involved the measurement of thermal resistance of the package. The forward voltage of the LED was considered as the temperature sensitive parameter. The thermal resistance measurement standard for LED packages, JEDEC 51-51 was used as the reference for this study. The junction temperature measurement principal is explained in detail in appendix D. A schematic diagram of the experimental set up is provided in Figure 33**.**

The first step of the measurement process is calibration. The goal of the calibration is to obtain a relationship between junction temperature and forward voltage. The LED package is attached to the thermo-electric cooler using mechanical screws. The applied calibration current is 1mA. An explanation as to the choice of this current is provided in appendix D**.** The cold plate temperature of the thermo-electric cooler was increased from 25^0C to 75^0C in 5^0C increments. At each temperature setting, the LED was allowed to thermally stabilize and forward voltage across the LED was measured. The thermal stability criterion was that the standard deviation between five consecutive case temperature readings measured at every 1min interval should be less than 0.1^0C. An example of a calibration curve measured for an LED package is given in Figure 34. The gradient of the calibration curve is referred to as the K-factor.

The next step is to measure junction temperature at the operating current of 1A. The cold plate temperature was set at 25^0C. The LED was allowed to thermally stabilize at an operating current of 1A, as per the stability criterion mentioned above. Once the system

reached thermal stability, the operating current was changed from 1A to 1mA. The forward voltage of the LED was captured at 1mA current, after a 100µs delay and was averaged for 200µs duration. The extracted voltage is converted to junction temperature using the formula below.

$$T_j = \frac{(V_H - V_M)}{K}$$

Where, V_H – extracted voltage after junction heating, V_M – extracted voltage at measurement current before junction heating, and K – calibration factor

The case temperature is measured using a T-type thermo couple attached to the MCPCB, at a point closer to the substrate. The input electrical power was measured by measuring operating voltage and current, after the LED package reached its thermal stability. The following formula was used for electrical input power calculation.

$$P = V \times I$$

Where, V- voltage and I-current

The thermal resistance was determined using,

$$R_{\theta J-C} = \frac{(T_j - T_c)}{P_e}$$

Where, $R_{\theta J\text{-}C}$ – measured thermal resistance, T_j – junction temperature, T_c – case temperature, and P_e – electrical input power

This formula doesn't consider the optical power emitted by the LED. The optical power measured for this package at 1A, is 430mW. This would mean it has a quantum efficiency of 12% at 1A. If optical power was considered then the thermal resistance change will be smaller. However, electrical-to-thermal conversion ratio is smaller for this LED package at 1A, to have a significant impact on the measured thermal resistance value.

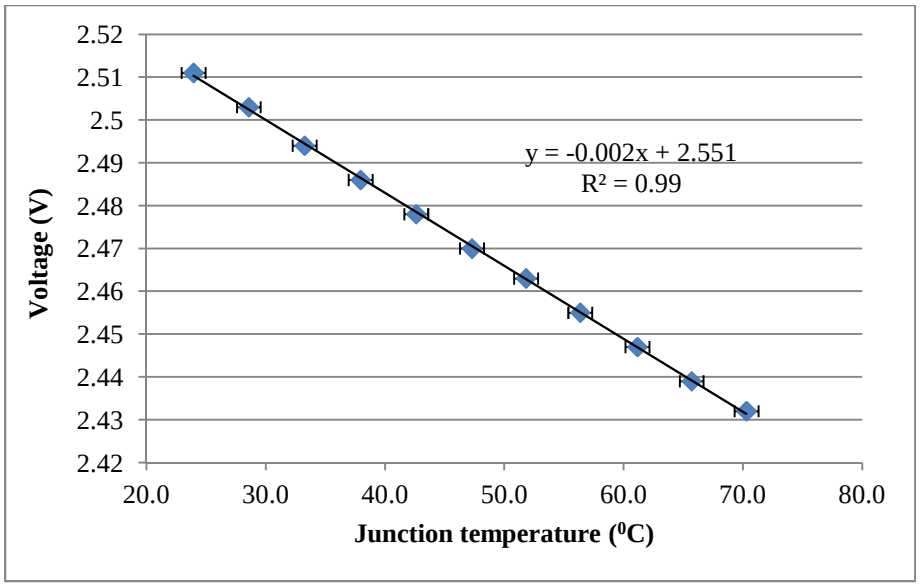


Figure 34. Calibration curve for junction temperature measurement for an LED package sample

3.4 Results

The measured junction-to-case thermal resistances at different stress conditions are plotted as a function of time. The variations of thermal resistance at different junction temperatures are plotted in Figure 35. The averages of five samples are plotted, except in the case of 448K condition, where only three samples were used. The time axis is normalized to the time at which the last measurement point was measured prior to failure. The absolute data prior to normalization is given in appendix F. The error bars include standard error of the mean within the group and measurement error. An analysis on measurement errors of thermal resistance measurements are given in appendix G. A large increase in thermal resistance was observed at 448K condition just before failure.

The variations of thermal resistance at different current densities are given in Figure 36. The averages of five samples are plotted, except in the case of 355A/cm^2 condition, where only an average four samples were possible. A sample at this condition showed an open circuit failure with a large increase in thermal resistance, at the point of failure. All other samples at all three current conditions showed short circuit failure. The initial spike in thermal resistance can be attributed to the expansion and subsequent relaxation of micro-voids in the thermal path due to application of stress. This is a short term, stress dependent phenomenon, which was only observed in the initial stage. The focus of this dissertation is permanent, irreversible degradations that occur in LED packages.

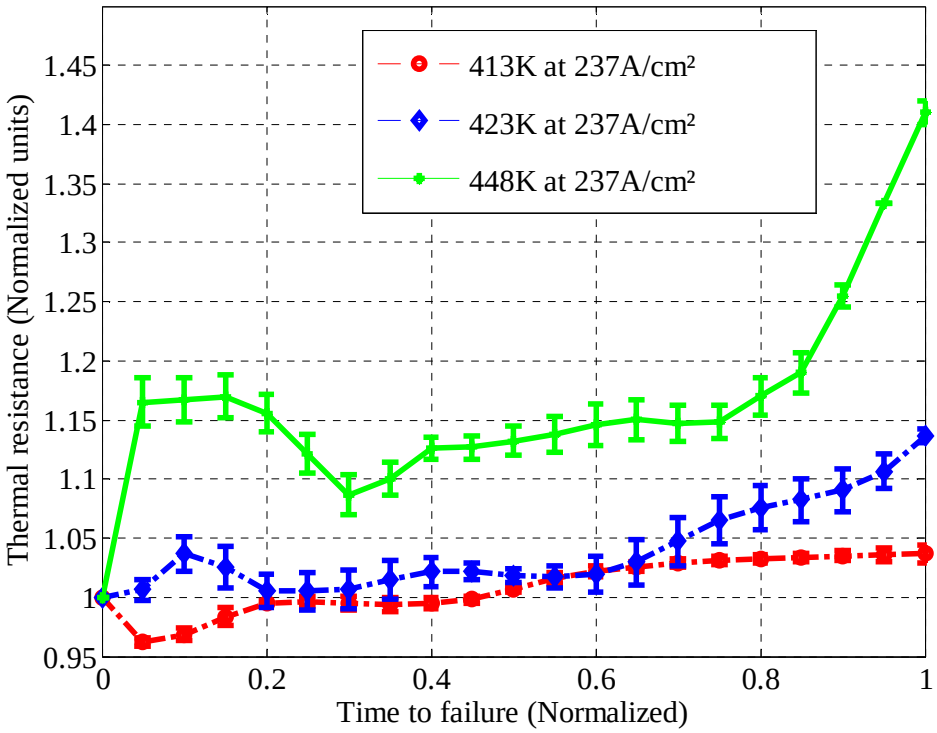


Figure 35. Variation of thermal resistance with time at different junction temperatures

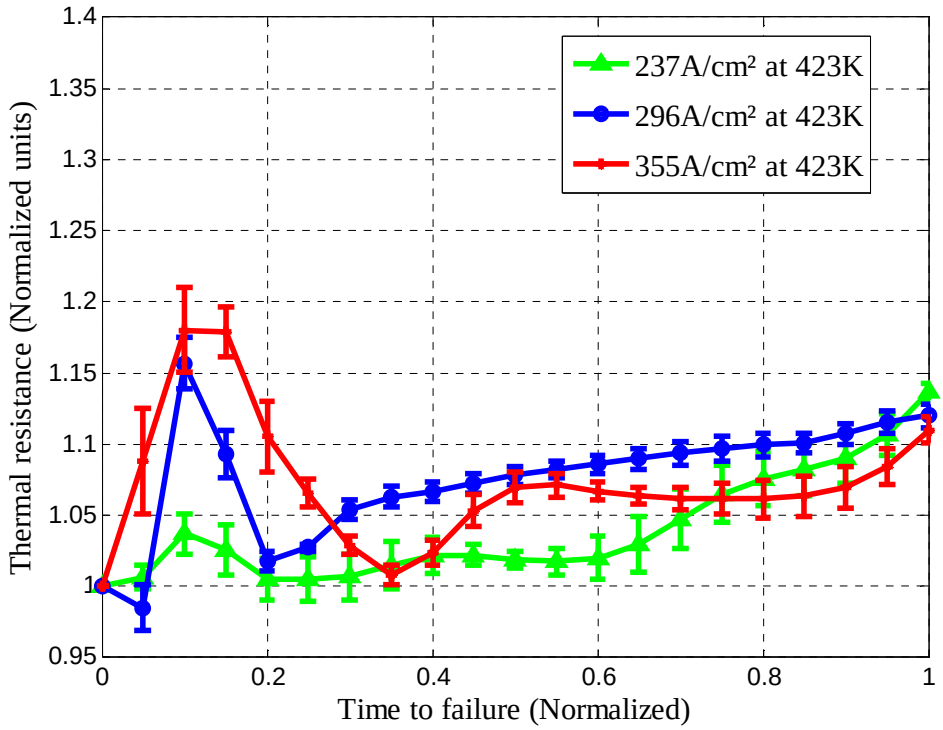


Figure 36. Variation of thermal resistance with time at different current densities

3.4.1 Stress calculation at thermal interfaces

In the literature review section 3.1, it was established that the thermal interfaces are subjected to highest stress within an LED package. Therefore, it is the degradation at the thermal interface layer that contributes towards junction-to-case thermal resistance increase. There are two thermal interfaces in this package, die-submount and submount-substrate. A stress calculation is performed for these two interfaces using an analytical stress analysis model, for a tri-material assembly [142]. The material properties used for the analysis is give in Table 3.

Table 3. Material properties

Material Property	GaN [143]	Si [144]	Alumina ceramic (A1- grade) [145]	$Au_{80}Sn_{20}$ solder[146]
Thermal conductivity (W/mK)	130	130	30-40	57
Melting point (^{0}C)	2500	1412	1700	280
Thermal diffusivity(cm^2/S)	0.43	0.8	0.12[1]	0.26[2]
CTE (1/K)	3.17e-06	2.6e-06	5.4e-06	1.6e-05
Thermal capacity (J/kgK)	490	700	775	150
Bulk modulus (GPa)	210	98	165	88
Youngs' modulus (GPa)	181	185	410-380	68
Poisson number	0.35	0.26	0.27-0.24	0.41
Shear Modulus (GPa)	67	52	164-158	25

Notes:

1. Calculated based on a density of 3.85 g/cm^3
2. Calculated based on density of 14.7g/cm^3

The analytical model considers forces due to thermal contraction, shearing force at the interface of two materials, and bending momentum in determining the stress on the thermal interface. The assumptions made by the model are,

- It’s a two-dimensional stress analysis model,
- Three material layers are equidistant, rectangular, and symmetrical layers,
- The term that accounts for non-uniform distribution of shearing forces, assume that the corrections are proportional to only the shearing stresses in the cross-section, and
- non-linearity effects of solder is not considered.

The displacement of a material layer due to these forces can be written as [142],

$$u(x) = \alpha \Delta t x + \lambda \int_0^x T(\in) d \in + \beta \tau(x) + \frac{h}{2} \int_0^x \frac{d\epsilon}{\rho(\epsilon)} \quad \text{equation K}$$

Where, α – coefficient of thermal expansion, t-temperature, λ – axial compliance, β – interfacial compliance, τ – shearing stress at the material interface, h – thickness of the material, and ρ – radius of curvature

The solution to the above equation has the form,

$$\tau(x) = Csinh(kx).$$

Where, k- Eigen value, x – distance from the center of the material layer, and C – constant

The eigen values and constants are determined by solving equation k for tri-material layers. The determination of C and k is explained in appendix H**.** The stresses at the two thermal interfaces are calculated at three different current densities. The different current-densities cause different temperature gradients; therefore, different stresses at the thermal interface. The stress distribution along the cross-section of the interface between the submount (Si) and substrate is given in Figure 37. The thermo-mechanical stresses are highest at the corners as reported in previous FEA studies [126], [128], [137]. The calculated average thermo-mechanical stresses are comparable to values reported in these studies for similar temperature gradients. The average stress values computed for two thermal interfaces are given in Figure 37. The stresses are highest at the submount-substrate interface; because, thermal expansion coefficient mismatch, and thermal resistivity is highest at this interface.

Table 4. Average stresses at thermal interfaces

Currents (A)	Temperature gradient (^{0}C)	Stress at die – submount interface (MPa)	Stress at submount – ceramic substrate (MPa)
1	55	46	107
1.25	75	65	145
1.50	100	85	194

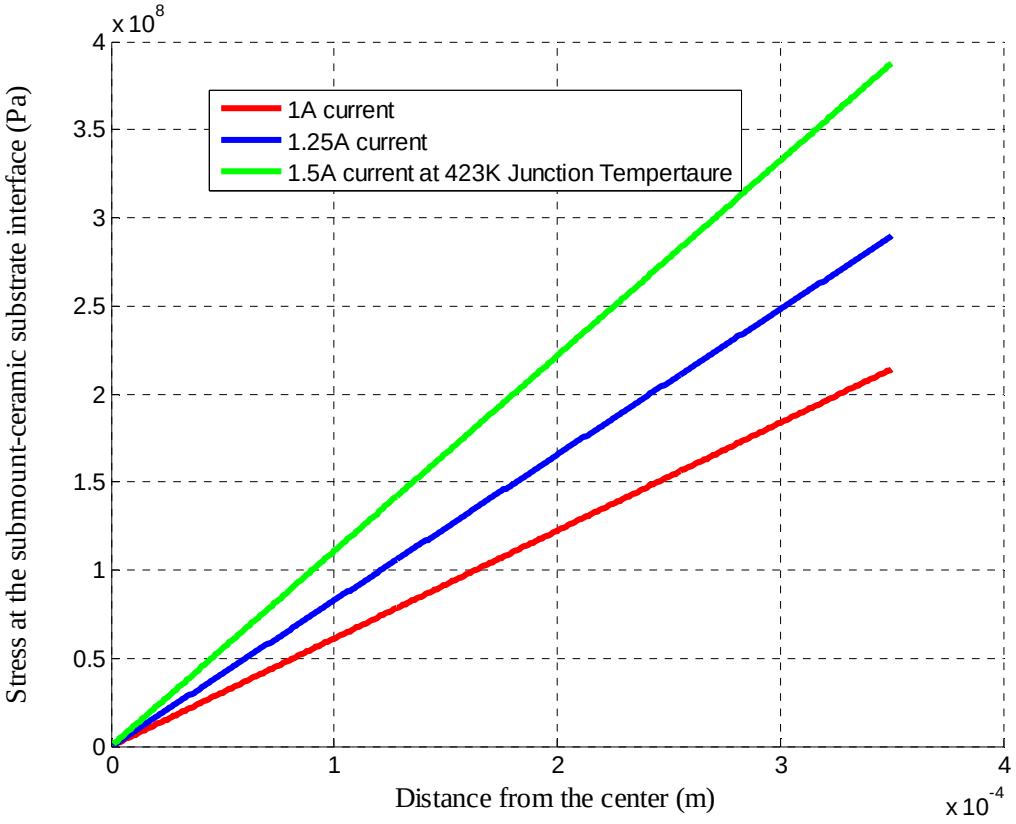


Figure 37. Stress at the submount-substrate interface as a function of distance from the center

3.4.2 Creep and thermal resistance change rate

Change in thermal resistance with time depends on formation of voids and cracks in the thermal interface layers. The formation of voids and cracks in the interface layers occur primarily due to stresses that are acting on the thermal interface layer. The high yield strength of these materials would mean that rather than abrupt failure, the material will undergo gradual degradation with time. The thermal interface layer is susceptible to creep induced plastic deformation. The creep strain is responsible for formation and growth of voids and cracks that is being filled with air. The air filled voids and cracks increase thermal resistance. In addition to thermo-mechanical stresses, creep is assisted by high temperatures that are closer to melting temperature of the die-attach solder.

The homologus temperatures of $Au_{80}Sn_{20}$ and Sn-Ag-Cu solder, at the three operating junction temperature conditions for this experiment is given in Table 5. The melting point of the $Au_{80}Sn_{20}$ solder is 280^0C and melting point of Sn-Ag-Cu solder is 220^0C [147], [148]. As a rule of thumb, for metals at homologous temperature greater than 0.5, creep becomes a dominant plastic deformation mechanism. Therefore, it could be concluded

that creep is the dominant deformation mechanism in this experiment. The creep deformation is assisted by both temperature and thermo-mechanical stress. Therefore, it could be argued that, thermal resistance change rate is proportional to creep strain rate.

Table 5. Homologus temperature of $Au_{80}Sn_{20}$ and Sn-Ag-Cu solder

Junction temperature (K)	Case temperature (K)	Homologus temperature $Au_{80}Sn_{20}$ solder	Homologus temperature Sn-Ag-Cu solder
413	358	0.75	0.73
423	368	0.76	0.75
448	393	0.81	0.80

Thermal resistance change rate was calculated for each sample at all different conditions. The Dorn-Weeterman power law given in equation J, proposed a relationship between creep strain rate with stress and temperature. The creep strain rate in this equation referred to steady state creep strain rate. Therefore, transient or short term changes of creep strain at the initial or rapture stages are not considered. An example of steady state thermal resistance change rates extraction from measured thermal resistance data is given in Figure 38.

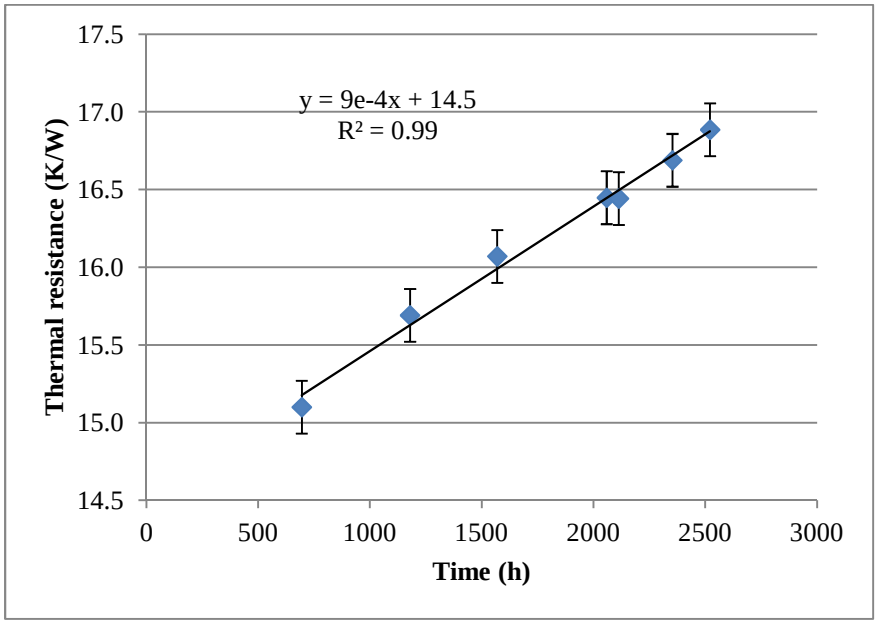


Figure 38. Steady state variation of thermal resistance for an LED package at 296A/cm^2 current density and 423K junction temperature

When the driving current is constant, the temperature gradient within the package is also constant; therefore, the thermo-mechanical stress is constant. At iso-stress conditions the Dorn-Weeterman power law can be written as,

$$\dot{\epsilon} = C exp\left(\frac{-Q}{RT}\right).$$

Where, Q – activation energy, R – universal gas constant, T – temperature, and C – constant

The thermal resistance change rate at different case temperatures were plotted in Figure 39. The data points represent the average of thermal resistance change rate for samples at each temperature stress conditions. The stress calculations in 3.4.1 showed that thermo-mechanical stress is highest at the submount-substrate interface. It is reasonable to assume that the thermal resistance increase is dominated by the degradation at this interface. The case temperature is a better indicator of temperature at this interface. As expected, the case temperature has a higher correlation with the thermal resistance change rate data.

The calculated thermal activation energy from Figure 39 is 52±3kJ/mol. A study that subjected $Au_{80}Sn_{20}$ solder to tensile stress reported an activation energy of 102kJ/mol [149]. The LED package used for this experiment used $Au_{80}Sn_{20}$ type solder at the die-submount interface. The type of solder used in the submount-substrate interface is not known. However, it is known that the solder is lead free and contains Ag, through energy dispersion spectroscopy. The bonding pad on the ceramic is Cu. Even though the exact composition of the solder is not known, it is reasonable to assume it's a Sn-Ag-Cu compound. Further, this is a popular lead free solder compound used in the electronic industry. The reported stress independent activation energies for creep deformation for Sn-Ag-Cu solder range from 39-83kJ/mol [147], [148], [150], [151]. The calculated activation energy is lower than the activation energy for creep deformation in $Au_{80}Sn_{20}$ solder, but is within the reported range for Sn-Ag-Cu solder. This is further validation that creep deformation is predominant in the submount-substrate interface. In order to identify the deformation mechanism in the solder layer the stress exponent must be calculated.

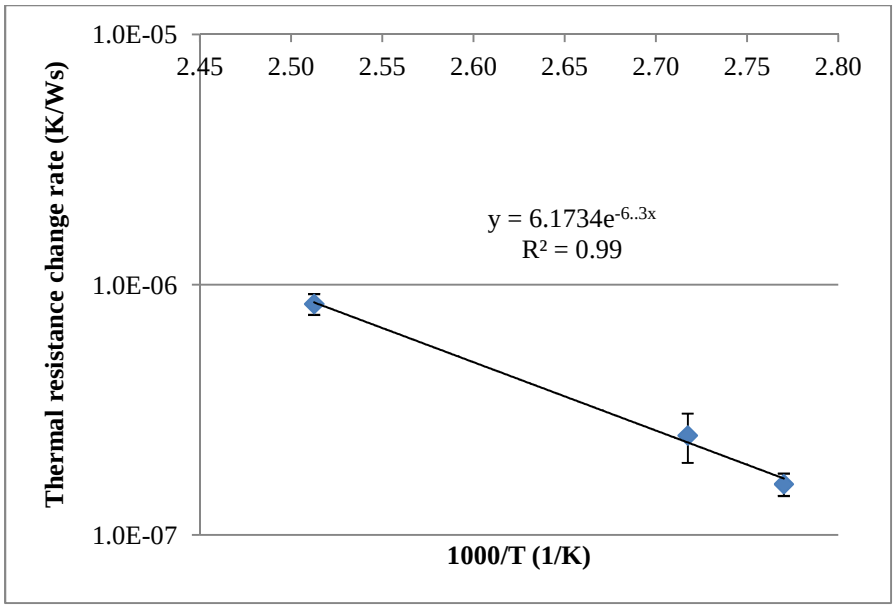


Figure 39. Thermal resistance change rate at different case temperatures

The experiment that kept junction temperature constant, while varying the driving current is used to calculate stress exponent. At constant temperature the Dorn-Weeterman power law can be stated as,

$$\dot{\epsilon} = B\sigma^n$$

Where, B – constant, σ - the applied thermo-mechanical stress, and n-exponent

The variation of thermal resistance at different operating currents is given in Figure 37. The average stresses at the surmount-substrate interface at different currents, calculated in section 3.4.1 were plotted against the thermal resistance change rate in Figure 40. The results suggest that the applied thermo-mechanical stress didn't have any impact on thermal resistance change rate. In other words an increase in applied stress didn't result in an increase in creep strain. This observation is not in line with creep deformation studies that were performed on different material systems.

In the analysis of the activation energy it was shown that case temperature had a strong correlation with thermal resistance change rate than junction temperature. This is because case temperature is a better indicator of temperature for the submount-substrate interface. In the experiment case temperature was not kept constant. At higher currents, the case temperature was cooled down to maintain constant junction temperature. Therefore, it could be argued that it is the net effect of high current (high stress) and low temperature that is shown in Figure 40. Therefore, if the thermal resistance change rates are adjusted

for low case temperatures, then they should show a conventional power law relationship with applied stress.

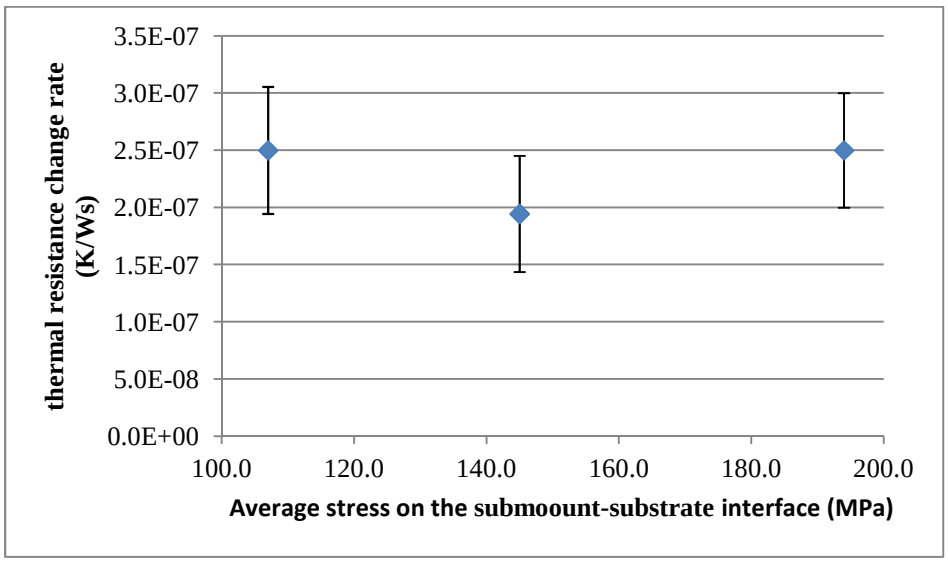


Figure 40. Variation of thermal resistance change rate with thermo-mechanical stress

The expected thermal resistance change rate at a given case temperature was estimated using the temperature and thermal resistance change rate relationship in Figure 39. This relationship is only valid for the thermo-mechanical stress condition of 107MPa. Therefore, the expected thermal resistance change rate value given in Table 6 is calculated for a stress condition of 107MPa. The measured values are higher than the expected value, due to the increase in stress. The ratio of measured value over expected value is plotted with the stress increase in Figure 41.

Table 6. Calculation of thermal resistance change rate increase due to thermo-mechanical stress

Stress (MPa)	Case Temperature (K)	Expected value (K/Ws)	Measured value (K/Ws)	Increase due to stress	Uncertainty
107	368	2.5e-7	2.5E-07	1	±0.1
145	348	9.5e-8	1.9E-07	2	±0.4
194	323	2.1e-8	2.5E-07	12	±1.0

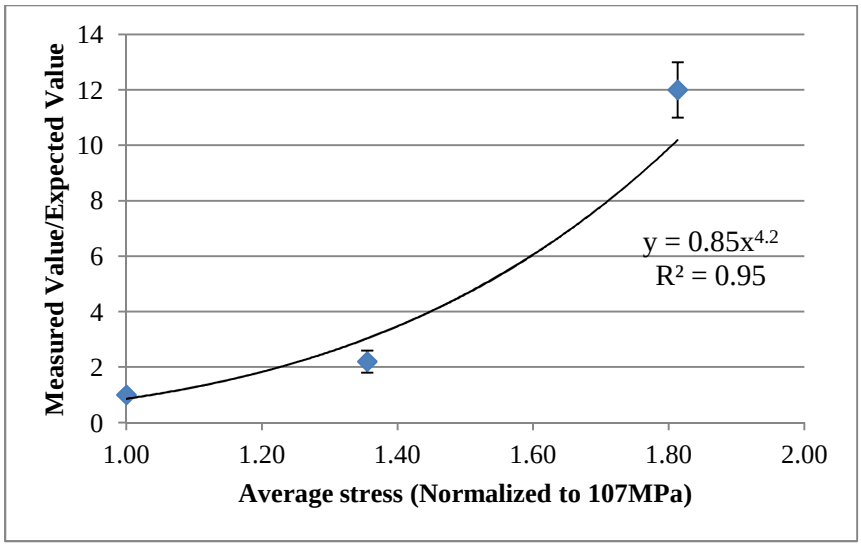


Figure 41. Thermal resistance change rate increase due to applied stress

The measured stress exponent for this experiment is 4. The measured stress exponents for Sn-Ag-Cu solder range from 4-13 depending on the stress conditions [147], [148]. At low stress regimes the reported stress exponents were between 4 and 5. The calculated stresses at the interface can be called as lower stresses, when compared with the stresses used in previous studies. The calculated stress exponent agrees well with the reported values in literature for the stress conditions used.

The stress exponent indicates evidence with regard to the creep mechanism experienced by the material [152], [153]. Diffusional creep dominates when stress exponent is one [154]. Diffusional creep occurs due to the stress directed flow of vacancies in grain boundaries. This mechanism is predominant in low stress high temperature conditions. The stress exponent closer to 2 suggests that grain boundary sliding is the dominant creep deformation mechanism [149], [155]. The large stress exponent values (4 -13) reported in literature for different alloy systems is explained using dislocation creep mechanism [152], [153].

Dislocations in a lattice move along the lattice deforming the lattice and the material. The plane that a dislocation moves along a crystal is referred to as a glide plane. The movement along the glide plane is triggered mainly by the applied stress. The glide motion is responsible for the strain in the material [152], [153], [156], [157]. However, dislocation movement is constrained by the presence of point defects and grain boundaries. The dislocation climb plays a critical role in such instances to facilitate continuous movement of dislocations. The dislocation climb depends on the diffusion rate of vacancies. Therefore, the velocity of dislocation movement in a material is controlled by temperature [152], [153], [156], [157]. Based on the stress exponent

calculated in this study, dislocation creep mechanism dominates the deformation of the Sn-Ag-Cu solder layer.

3.5 Chapter summary

Thermal resistance of an LED package is an indicator of the quality of its heat conduction path. The heat generated in the junction is conducted via submount, thermal interfaces and substrate to ambient. The degradation of thermal path will lead to an increase in thermal resistance and therefore, the junction temperature. LED package reliability studies have observed an increase in thermal resistance with aging. These studies have attributed delamination in die-attach layer as the prime cause of thermal resistance increase. Finite element analysis studies have corroborated this hypothesis by showing that the highest stress parts of the package are its thermal interfaces, and void formation at the interface has a direct correlation with thermal resistance increase.

The delamination occurs in the die-attach layer primarily due to thermo-mechanical stress. The thermo-mechanical stresses occur due to the CTE mismatch between different material layers. The fundamental cause of plastic deformation creep strain. Therefore, it is reasonable to assume that creep strain rate is proportional to thermal resistance change rate. Thermal resistance change rates of a package could be easily measured over time, while it is difficult to measure creep strain rate of material layers when they are packaged. If thermal resistance indeed has a correlation to creep strain, then thermal resistance change rate must follow the Dorn-Weteerman power law.

The study measured thermal resistance change rate of a GaN-based LED package at different current and junction temperature stress conditions. Following important observations were made in this study.

- Thermal resistance change rate follows the Dorn-Weeterman power law. At high junction temperature conditions thermal resistance change rate is also higher. However, better correlation was observed with case temperature rather than with junction temperature.
- The thermo-mechanical stress is highest at the surmount-substrate interface. The case temperature is a better indicator of temperature at this point. It is the degradation at submount-substrate interface that is responsible for thermal resistance change with time.
- Thermal resistance change rate also depend on the operating current. At higher operating currents the thermal interface experiences large temperature gradients; therefore, large thermo-mechanical stresses.

- High stress exponent of 4 suggests that dislocation creep is the dominant creep mechanism. The glide motion of dislocations is responsible for creep strain. However, the dislocation velocity depends on dislocation climb. The dislocation climb depends on vacancy diffusion; therefore, on temperature. The measured activation energy of diffusion is 52kJ/mol. The reported stress exponent and activation energy agrees well with the reported values for Sn-Ag-Cu solder at similar stress conditions.
- These model parameters would enable a-priori estimation of die-attach life time based on creep deformation.
- The open circuit failure of LED packages occurred due to delamination at the submount-substrate interface. These delamination causes rapid increase in thermal resistance at the point of failure, that increases the die-attach solder temperature up to its meting point.

4 Fault detection and prediction

This chapter will present a discussion on failure analysis of LED packages by combining the experimental evidence presented in chapters 2 and 3. The failure analysis would also use post-mortem analysis to eliminate failure possibilities. This section would reinforce the hypotheses with regard to failure mechanisms discussed in greater details in chapters 2 and 3. This chapter would also present a brief discussion on data driven and physics of failure based approaches that could be employed to both detect and predict failure in LED packages. The experimental evidence presented in the thesis is applied to detect, and predict failure.

4.1 Failure analysis: short circuit failure

Failure mechanisms that could cause short-circuit failure in an LED package, along with the change in electrical and thermal parameters that may have occurred as a result of such failure mechanisms are summarized in Table 7. The metal/impurity diffusion into the semiconductor die failure mechanism is explained in detail with supporting experimental evidence, in chapter 2. In the same chapter it was explained that metal atoms for diffusion is provided by electromigration at the contact metallization. The other two failure mechanisms and why they didn't occur in this study is briefly explained in this section.

Table 7. Short circuit failure mechanisms

Failure mechanism	Detection parameter
Metal/impurity diffusion in semiconductor die	Series resistance decrease Ideality Factor increase Reverse leakage current increase
Conductive filament formation at the substrate	Increase in current in the low bias region Increase in reverse leakage current
Die-electric passivation layer breakdown	Reverse leakage current increase

Conductive filament formation between negative and positive pad could lead to short circuit failure. The conductive filament formation is observed PCBs used in electronic circuits. The key factor that facilitates this phenomenon is the formation of a path between two conducting traces [97]. This path creation and metal migration along this path is also referred to as electrolytic electromigration. If this failure mechanism occurred then the insulation resistance between two metal pads should be lower. However, the

measured resistance between the positive and negative contact pads after failure suggested that the insulation between the two pads remained intact.

The breakdown of passivation/di-electric layer is an identified reliability issue in SiC based high power devices such as MESFET, SITs, etc. [94], [95]. The breakdown of passivation layer depends on the temperature and applied electric fields. The die-electric layer breakdowns were observed at electric fields greater than 5MV/cm and at temperatures greater than 250^0C. The stress conditions used in this study is nowhere near these high stress conditions. Even if there is a die-electric layer breakdown, the catastrophic short circuit failure is possible only in LED package types such as flip-chip and thin film vertical structures. It is hard to predict an alternative current path that would bypass the junction in the vertical LED package structure that is used in this study.

4.2 Failure analysis: open circuit failure

Experimental evidence suggests that there are two main plausible explanations for open circuit failure.

- The electromigration induced void formation in the wire-bond at the cathode, leading to wire-bond failure.
- Thermal fatigue induced delamination leading to high die temperatures.

Open circuit failure was observed in all samples that operated at 448K and 237A/cm^2 stress condition. Experimental evidences that support electromigration induced void formation as the failure mechanism are,

- continuous increase in series resistance, and
- browning around the cathode wire-bond.

However, this failure mechanism cannot explain the large increase in thermal resistance that occurs just before catastrophic failure. If the series resistance change profile in Figure 19 and thermal resistance change profile in Figure 35 is compared, the rate of change of both series resistance and thermal resistance increase rapidly at the last 20% of its life. Further, void growth in the cathode will not cause a thermal resistance increase, as the, the cathode doesn't play a prominent role in heat dissipation.

The LED package samples were dipped in dichloromethane (CH_2Cl_2) to dissolve the epoxy lens and silicone encapsulant for 24 hours. In LED package samples that showed open circuit failure, the die was detached from the substrate. Since this detachment from substrate occurred only in the case of packages that had open circuit failure, the only plausible explanation is that there is significant delamination at this layer during aging. The microscopic examination of substrate showed significant damage at the solder layer.

At the point of failure, the melted die-attach solder overflowed from the cathode point. The measured thermal resistance of an LED package just before open circuit failure was 32K/W. This would mean that at a current of 1A the junction temperature of the LED package is approximately 260^0C. The melting point of $Au_{80}Sn_{20}$ solder, die-attach material used in this package, is 280^0C. This further proves the fact that die-attach solder melted at the point of failure leading to delamination.

The delamination would have occurred over a period of time and would have created localized temperature gradients within the package. The wire-bond at the cathode has the highest current density in the package. Therefore, localized temperature at this point is higher than at any other point in package. The die-attach solder at the vicinity of this point may have reached the melting point first and the consequent pressure build up caused the solder over flow at this point.

When the LED package is allowed to sufficiently cool down and powered back on, the LED will function momentarily and turns-off after a little while. As long as the heat generated in the junction doesn't increase the die-attach solder temperature closer to its melting point, the package will function. To illustrate this further, the LED package was attached to a thermoelectric cooler and an IV sweep was performed at two different temperatures. The current-voltage characteristic curves at 25^0C and 75^0C are given in Figure 42. When case temperature is maintained at 25^0C, both current and voltage shows stability. However, at a temperature of 75^0C, there is discontinuity in I-V curves, at currents above 100mA. This further proves the electrical contact discontinuity that occurs due to die-attach solder meltdown. All these evidence suggests that the reason for open circuit failure is the delamination at the die-attach layer.

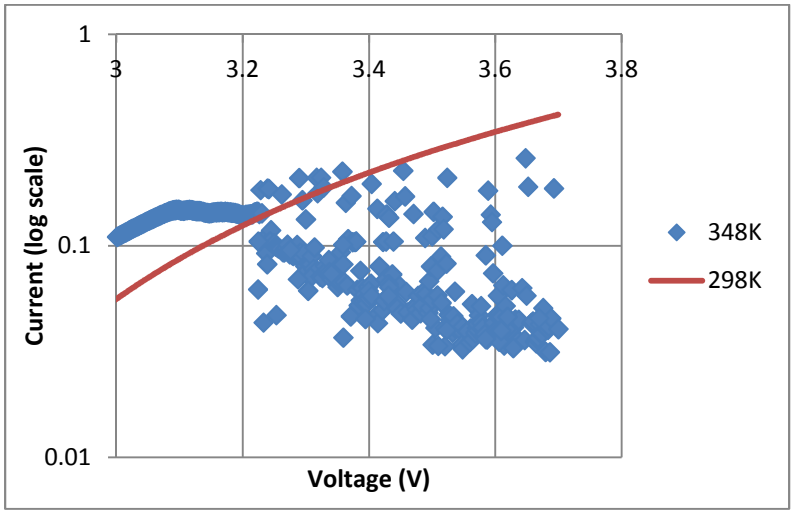


Figure 42. The current-voltage characteristics of an LED package with open circuit failure

4.3 Fault detection

Fault detection involves identifying that a fault has occurred in the system, so that corrective action could be initiated. Depending on the complexity of the sensor network, fault isolation is also possible. Fault detection and diagnostics algorithms are widely used in many different applications ranging from military, medical equipment, production facilities, servers, personal computers, etc. There is an emerging trend in the lighting industry to incorporate fault detection in lighting applications.

In lighting systems catastrophic fault detection can be done using Euclidian distance method [29], [158]. Non-optical, easy to sense parameters such as voltage and case temperature could be used for this purposes.

$$ED = \sqrt{(V - V_{mean})^2 + (T - T_{mean})^2}$$

Where, V – voltage and T – case temperature

The mean values can be established using a training algorithm at the initial phase of operation. Different layers of complexities could be added to the algorithm. The main advantage of this approach is that the computational power required in in-situ applications is limited. However, this approach cannot discriminate between fault modes.

The measured ED values for an LED package over its life are given in Figure 43. The fault can be detected by setting a threshold. There are two instances that the ED values cross the fault line. The first instance is due to wire coming off from solder-pad and the second instance is the LED package failure. This method can detect faults when it happens, but cannot discriminate between different failure mechanisms.

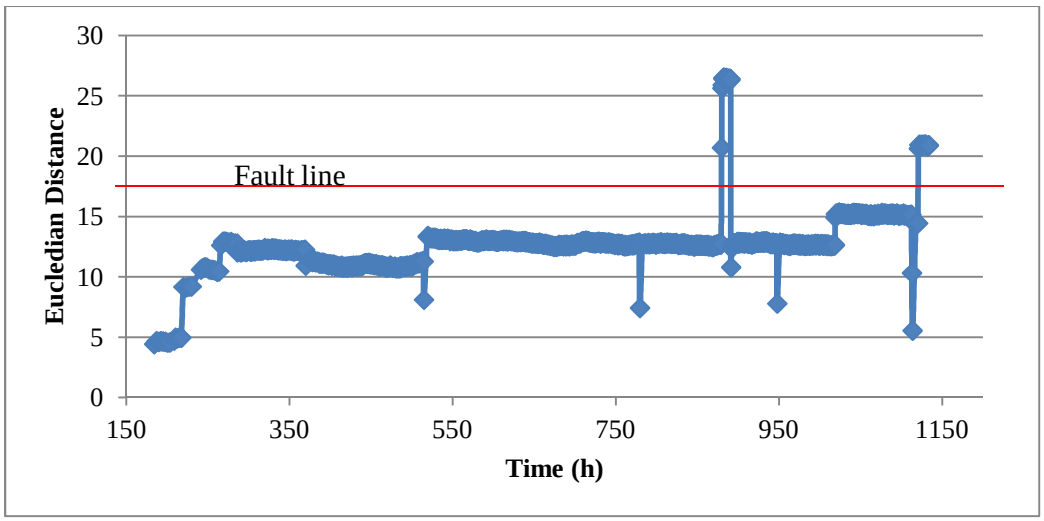


Figure 43. Fault detection of an LED package using Euclidean distance approach

4.4 Fault prediction

Fault prediction involves real-time estimation of remaining useful life, in a given application. This approach is superior to fault detection in its ability to provide a warning to the user about the impending failure of a system. However, to implement fault prediction in depth understanding of failure mechanisms are required. Prognostics and health management (PHM) is a method that "permits the assessment of the reliability of a product or system under its actual application conditions [29]." There are two main approaches to PHM, physics of failure based approach and data driven approach.

4.4.1 Data driven approach

The data driven approach depend purely on sensor outputs to make predictions on system health. There are different statistical approaches and machine learning techniques that could be used to process the data and extract trends or special features within the data for health prediction purposes. However, to implement this method an understanding on stable and unstable regions with respect to the parameters being monitored is required.

A discussion on pros and cons of different algorithm options are beyond the scope of this thesis. The thesis provides information on change of electrical and thermal parameters with time up to the point of failure. Product development engineers could decide on the most efficient pattern recognition algorithm that could detect the pattern at the point of failure. Data driven algorithms can be categorized as,

- parametric statistic approaches (ex: minimum mean square error estimation, likelihood ratio test, etc.),
- non-parametric statistic approaches (ex: nearest neighbor-based classification, chi-square test, Kolmogrov-Smirnov test, etc.), and
- machine learning.

There are several approaches to apply a data driven approach to this study. In section 2.7.4, a physics based resistance change equation was developed for LED packages that showed short circuit failure. The constants A, C and b can be calculated using a training algorithm. It is shown in the physics based model that A and b depends on temperature. A pattern recognition algorithm could detect the pattern of resistance change and give an indication to the user.

$$R(t) = A \times t^{\frac{-1}{2}} \times \exp\left(-\frac{b}{t}\right) + C$$

Open circuit failures can be easily detected by establishing an upper threshold for series resistance and thermal resistance. The experimental evidence at 448K suggests that

threshold criterion for 30% increase in thermal resistance or 50% increase in series resistance is adequate to provide advance failure indication to user. The slope change detection is another solution to indicate failure. The rate of change of series resistance increase by 3 times and rate of change of thermal resistance increase by 8 times before failure.

Another approach is to use an empirical relationship supported by experimental data. For example, Euclidean distance (ED) vector can be calculated for combined variation of series resistance and thermal resistance. The experimental data suggests that ED values follow a Gaussian function with time. There is no physics based explanation for this as the previous case, yet it is an empirical relationship experimentally verified. Figure 44, shows the variation of Euclidean vector distance with time, along with the Gaussian fit for a group of LED packages at 423K. The relationship between ED value and time could be stated as,

$$ED(t) = Aexp(-\frac{(t-b)^2}{c^2}).$$

Where, A = 0.22 ± 0.02, b = 0.69± 0.04, and c = 0.50±0.08

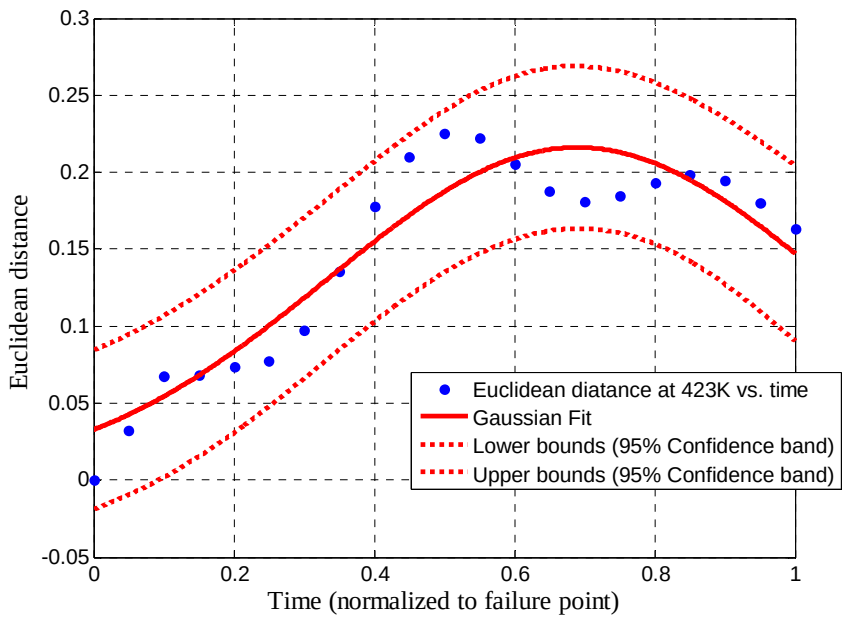


Figure 44. Euclidean distance for LED packages at 423K and 237A/cm^2 stress condition

In the above case an ED threshold and a failure criterion need to be established. The bounds for ED value could be set by defining the desired control criterion. One such criterion could be that the failure warning must be generated before the actual failure. This would help to determine the lower threshold for ED. The criteria that ED has to be a

real number could help to establish the upper threshold. In this example based on the defined criteria bounds, ED could be specified as, 0.15 < ED < 0.20. When the desired ED value is specified by the user, the remaining useful life (RUL) of this LED package can be calculated as, RUL = 1- t. If an ED threshold of 0.18 is specified with a negative slope detection criterion for the case in shown in Figure 44, user would receive a warning when the estimated remaining life of the LED package is less than 10% of its total life.

The disadvantage of this approach is that the sample size used to determine the parameters in the algorithm should be large. In order to predict failure at 10% remaining life condition with 95% confidence, two additional ED thresholds are required to cover lower and upper 95% confidence bound conditions. This would increase the complexity of the implementation. The threshold criterion is stress condition dependent; therefore, algorithm parameter calculation and threshold determination must be done at expected operating stress conditions. Prior to implementing this approach it needs to be verified whether the ED variation with time follows a Gaussian function for stress conditions other than the ones used in this study. In the case of 448K condition, ED variation with time didn't follow a Gaussian function. In this case ED increased continuously till the point of failure. However, it is easy to establish failure criterion for such patterns with high confidence using a single threshold.

In summary, two data driven approaches to predict failure is presented. One approach uses a pattern recognition algorithm to capture series resistance change with time to detect short circuit failure. To detect open circuit failures threshold or a slope variation criterion is used. These variation patterns are linked to physics of the underline failure mechanism. Another approach uses the variation of ED that is calculated using both series resistance and thermal resistance change data with time to capture failure. In this method short circuit failure is captured by three ED thresholds and a negative slope detection criterion. The open circuit is captured by using an ED threshold of 0.6 and a positive slope criterion.

4.4.2 Physics of failure based approach

The physics of failure based approach identify the fundamental failure mechanism and predict the life based on the stress conditions under real life operating conditions. There are numerous failure mechanisms that are possible in an LED package. A fault tree diagram with catastrophic failure mechanisms is provided in Figure 45. Every, failure mechanism in this fault tree have some finite probability of occurrence. The probability of occurrence might change depending on the stress conditions, the LED package type, manufacturing process, etc. In order to implement PoF-based approach in practical applications it is critical to know the failure mechanism/s with the highest probability of

occurrence, under a given range of stress conditions. It is critical in system design to be aware of this fact, when extrapolating these results into other stress conditions.

In this study the stress conditions used were current and temperature. The dominant failure mechanisms were,

- electromigration induced metal diffusion in to semiconductor, and
- creep strain induced thermal interface delamination.

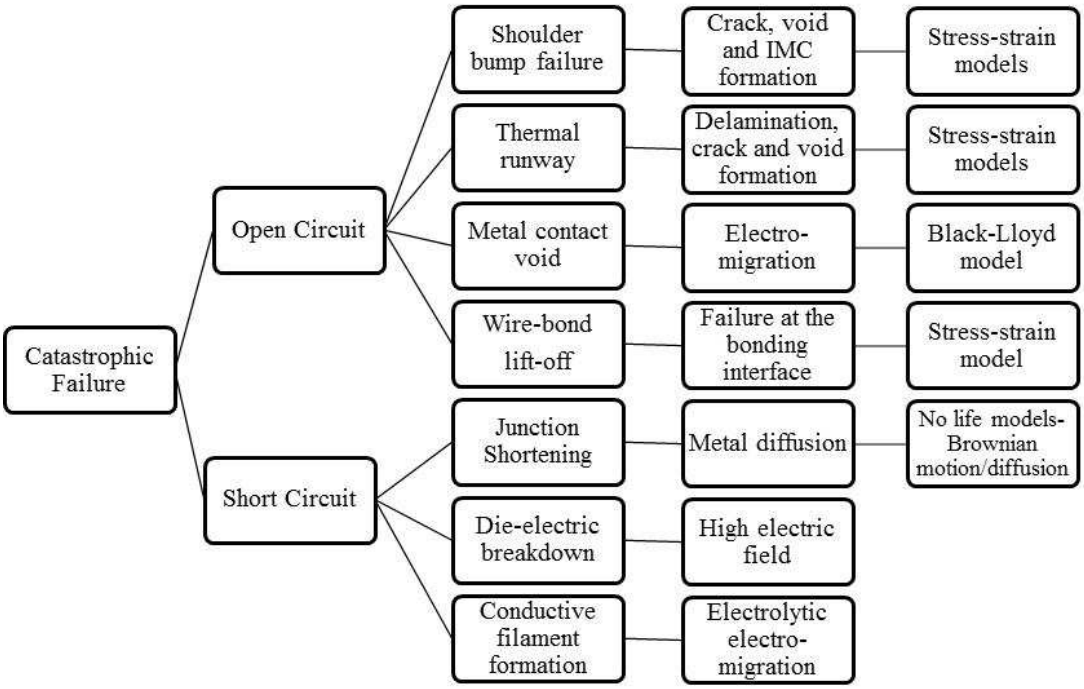


Figure 45. Fault tree diagram for catastrophic failure in LED packages

It is important to note here that in electromigration and diffusion of metal into semiconductor, two separate mechanisms are combined together. This is because the two mechanisms are interdependent. The series resistance change profile in Figure 22, captures the impact of both of these mechanisms. At different phases it was assumed that one mechanism dominates over the other. The basis for these assumptions and its implications in understanding temperature and current dependencies on these mechanisms are explained in sections 2.7.4 and 2.7.7. Even though metal spiking in to active region as a failure mechanism was observed in semiconductor packages, there is no known physics based life-time model to predict such failures. There is an empirical model developed by Black to predict electromigration failure time of a metal, which was later validated for specific cases by theoretical explanations.

The diffusion of atoms within a material is defined by Einstein's relationship and Ficks' laws of diffusion. It is logical to state that metal concentration increase in the junction would lead to failure. However, rate and nature of such diffusion is influenced by the location, orientation, and movement of dislocations in GaN. Molecular dynamic studies on GaN have showed that impurities prefer to diffuse along a dislocation in the crystal [51], [159]. Therefore, there is no obvious theoretical relationship between series resistance change or failure time with diffusion. One such attempt to develop a relationship between resistance and impurity concentration just before metal spiking in the junction is explained in section 2.7.4.

In absence of a theoretical model, empirical relationship was developed based on fundamental physics governing these two mechanisms for current and temperature stress conditions. Since both mechanisms depend on diffusion, using Einsteins' relationship, a mean displacement (x) of a particle in d-dimensional space can be stated as,

$$x^2(t) = 2dDt$$

Where, D- diffusion coefficient, and t – time

Arrhenius relationship is a good predictor of diffusion coefficient at different temperatures.

$$D = D_0 \exp\left(\frac{-Q}{kT}\right)$$

Where, Q – activation energy, T – temperature, D_0 – pre-exponent coefficient, and k – Boltzman constant

If the mean displacement of N number of particles of Au towards semiconductor leads to failure, the time to failure (T_f) can be stated as,

$$T_f \propto \frac{1}{D_0 \exp\left(\frac{-Q}{kT}\right)}.$$

The relationship between time to failure and different temperature conditions are plotted in Figure 46. The data points represent the mean time to failure for the samples at each condition, and error bars are the standard deviation within the group. In the case of LED packages at 448K, the time to failure was determined as, the time at which the series resistance increases up to 50%. The actual failure of these packages was caused due to creep rapture in the die-attach. Therefore, the time at which creep rapture was initiated was considered as the failure point. The actual failure point was considered for LED packages at other conditions, since they all fail due to diffusion of metal into semiconductor.

The extracted activation energy is 0.62eV. This activation energy must be interpreted with caution as this combines activation energies required for self-diffusion of Au and diffusion of Au into GaN. The activation energy measured in section 2.7.2, of 0.46eV is a better indicator of activation energy required for diffusion of vacancies in the contact metal. If the activation energy was measured only using two temperature points (413K and 423K), it comes to 0.23eV. This activation energy is closer to the reported activation energies (0.23eV – 0.28eV) of impurity migration along dislocations of GaN [159]. The failure mechanism is dominated by diffusion of Au along dislocations into GaN; therefore, it is reasonable to expect that activation energy is closely associated with this mechanism. Using activation energy of 0.23eV, the time to failure through metal diffusion for LED packages at 448K can be calculated as, 1648h. The die-attach delamination caused open circuit failure in package before metal migration could initiate short circuit failure.

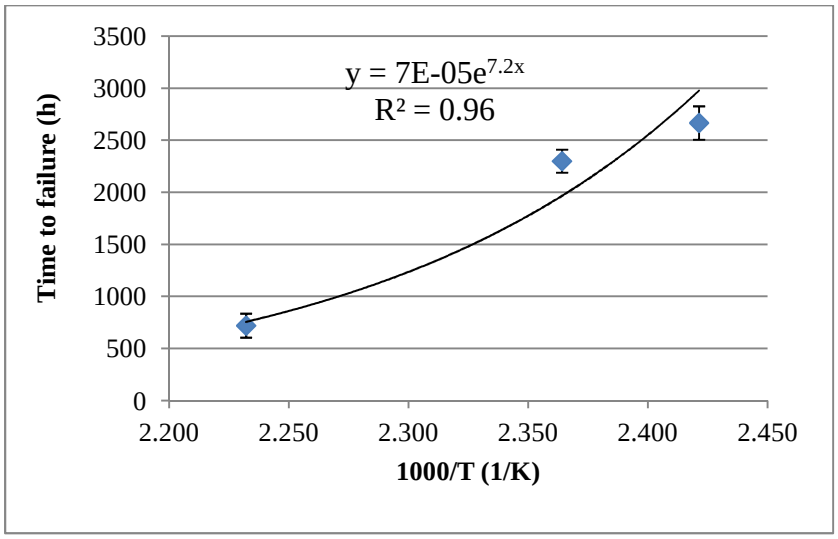


Figure 46. Failure time at different junction temperatures

The metal migration would lead to void nucleation and void growth. The metal migration process is directional, and it is reported in literature that Au atoms migrate in the direction of electron flow [106], [108]. The directionality to otherwise random movement of ions is induced by the force applied by current. The time to failure can be stated as,

$$T_f \propto \left(\frac{1}{j} + \frac{1}{j^2}\right)$$

Where, j – current density

The two terms represent void growth and void nucleation processes initiated by current in the contact metal. The mean time to failure is plotted as a function of different drive currents in Figure 47. The extracted A and B constants suggest that 60% of the total failure time is consumed by void nucleation process. This graph presents an interesting picture when compared with Figure 57. According to Lloyd [115], metal contacts that showed open circuit failure due to voiding showed the opposite. That is void growth phase became larger with failure time, whereas void nucleation phase remain constant. In the case of LED packages, the void growth phase remains constant, after the initial series resistance increase phase (phase 2), while void nucleation phase expand. The void expansion is limited by the bi-metal (Au/Ni) metallization layer. This explains why these packages didn't show a consistent increase in series resistance and showed open circuit catastrophic failure. The Ni layer may have acted as a barrier for further growth of voids.

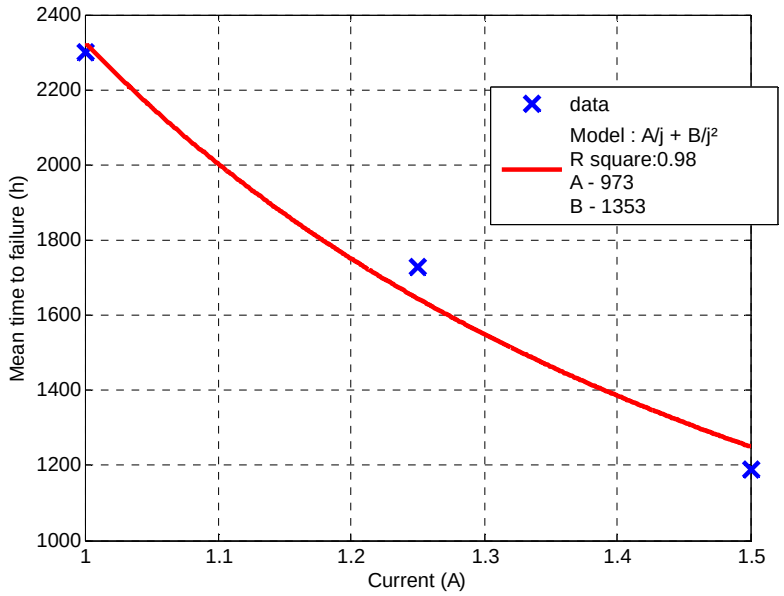


Figure 47. Time to failure at different currents

Two proportionality relationships can be used to develop a relationship for mean electrical metal contact life,

$$T_f = C \times \left[\frac{A}{j} + \frac{B}{j^2}\right] \exp\left(\frac{Q}{kT}\right)$$

Where, C is a constant that depend on material geometry, and diffusion length, A and B are constants that will depend on the proportion of void growth and void nucleation.

The other dominant failure mechanism is creep induced thermal interface delamination. It was stated in section 3.4.2 that steady state creep strain rate is proportional to thermal

resistance change rate of the LED package. This enables us to relate thermal resistance change rate with temperature and applied stress. The temperature in this case refers to the case temperature of the LED package.

$$\dot{R_{\theta J-C}} = K\sigma^{4.2}\exp\left(\frac{-52e3}{RT}\right)$$

The Monkmaan-Grant equation for creep rupture is stated as,

$$T_f = \frac{\in_f}{\dot{\epsilon}}$$

Where, $\dot{\varepsilon}$ – creep strain rate, ε_f – creep ductility, and T_f – time to failure

It was already established in previous chapter that creep strain rate is proportional to thermal resistance change rate; therefore, creep ductility can be calculated from Figure 48. The four samples that showed open circuit failure was used as data points. When creep ductility is known using the Monkmann-Grant model, the time to failure of the thermal interface could be determined. In real life applications LED packages are subjected to varying temperature conditions and cyclical loading conditions. The failure time in such cases could be determined through a combination of Monkmann-Grant and Palmgren-Miner rule as below [160].

$$N_f \frac{\sum_{n=1}^{N} \Delta t_n \, \dot{\epsilon}}{\in_f} = 1$$

Where, N_f - number of cycles to failure, $\dot{\varepsilon}$ – steady state creep rate, ε_f – creep ductility, Δt_n – time spent at a given stress level within a cycle, n – number of steps within the cycle, and ε_f – creep ductility

Using the above relationship we could write the number of days/cycles to failure of the thermal interface of an LED package in a lighting fixture as below.

$$T_f = \frac{2.7}{\sum_n^N \Delta t_n \dot{R_{\theta J-C}}}$$

If the stress conditions can be estimated before installation, then a-priori estimate of life can be obtained as below.

$$T_f = \frac{2.7}{A' \sum_n^N \Delta t_n [\sigma^{4.2} \exp\left(\frac{-52e3}{RT_{case}}\right)]}$$

The above equation can be further simplified using the relationship that,

$$\sigma \propto (T_j - T_{case}) = \Delta T$$

Where, T_j – junction temperature, and T_{case} – case temperature. This is a useful relationship, especially if life time estimations are done real time.

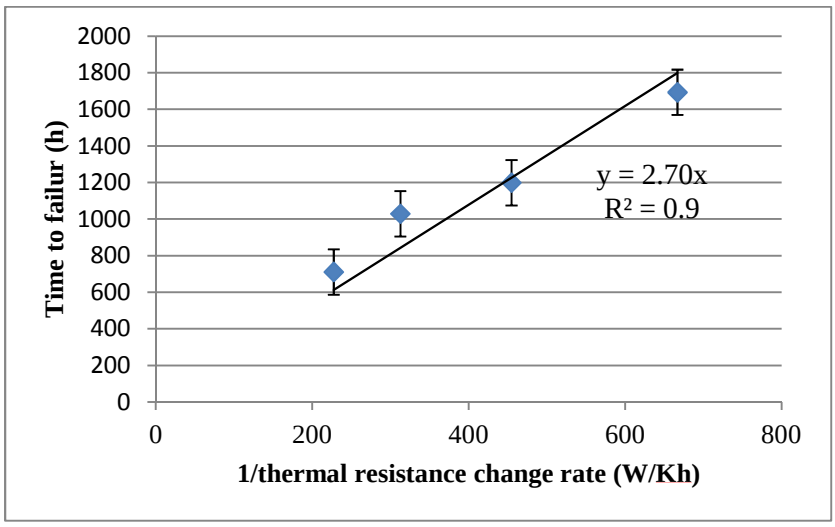


Figure 48. Creep ductility calculation

4.5 Combined physics of failure model for LED packages

The LED package is a system with different components such as, die, die-attach material, wire-bond, substrate, phosphor layer, and encapsulant. Failure of any one of these components would lead to system failure. Therefore, LED package could be viewed as a series system for reliability purposes where time to failure can be expressed as,

$$T_f = minimum[T_{f,die}, T_{f,die-attach}, T_{f,wire-bond}, T_{f,substrate}, T_{f,phosphor}, T_{f,encapsulant}]$$

The dissertation focused on catastrophic failure and demonstrated that at the stress conditions used in the study the dominant failure mechanisms were die failure due to electromigration induced metal diffusion, and die-attach interface failure. Therefore, above equation can be simplified as,

$$T_f = minimum[T_{f,die}, T_{f,die-attach}].$$

$$T_{f,die} = K \times \left[\frac{0.42}{I} + \frac{0.58}{I^2}\right] \exp\left(\frac{0.23q}{kT_{junction}}\right)$$

$$T_{f,die-attach} = \frac{2.7}{A \sum_n^N \Delta t_n [\Delta T^{4.2} \exp\left(\frac{-52e3}{RT_{case}}\right)]}$$

The time to failure data computed using the above model is indicated in Table 8.

Table 8. The predicted life times based on the model

Stress condition (Current/T_j/T_{case})	$T_{f,die}$ (h)	$T_{f,die\text{-}attach}$ (h)	Predicted time to failure (h)	Actual time to failure (h)
1A/413K/358K	2463	4740	2463	2667
1A/423K/368K	2128	2949	2128	2300
1A/448K/393K	1519	1000	1000	1090
1.25A/423K/348K	1980	2130	1980	1829
1.5A/423K/323K	1144	2556	1144	1190

The above model can give a-priori estimate of LED package life,

- if the stress conditions and their magnitudes are known,
- if the stresses are within the range of the stresses used in the dissertation, and
- if a similar package type with similar materials are used.

Further, research is required to validate whether this model can be used at stress conditions lower than the ones used in this study. It is known that mechanisms such as, void nucleation, and dislocation glide require certain threshold stress conditions. Therefore, if lower stress conditions cannot provide the required threshold then these failure mechanisms may not be significant. However, the presented model and the methodology adopted in deriving it shows great promise in predicting catastrophic failure of LED packages. This model should be viewed as a first step in developing a comprehensive life estimation model for GaN-based LEDs.

The uncertainty of the model prediction is evaluated using the propagation of error formula. The uncertainties of the model parameters (stress exponent and activation energy) determine the uncertainty of the life-time prediction. The activation energy is the dominant factor that determine the error in die failure time prediction, whereas stress exponent is the dominant factor in die-attach life time prediction. The details of the uncertainty analysis are given in appendix G. The model has a prediction uncertainty of ±110h for die failure and ±255h for die-attach failure.

The above model can be used to estimate life of an LED package real time in an application. This is useful when it is difficult to estimate the stress conditions that the LED package is subjected to before using it in an application. The real time estimation methods could provide reliable information, since they could adjust the initial projections in response to changes in stress conditions. A basic flow diagram of such a real time life projection strategy is demonstrated in Figure 49. The Eyrings' relationship is useful to calculate acceleration factors in response to changes in stress condition. The Eyrings' relationship states that,

$$AF = (\frac{\sigma_1}{\sigma_2})^n \exp\left[(\frac{E_a}{K})\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

Where, E_a – activation energy, n- stress exponent, T – temperature, σ – stress/current, and K –Boltzman/gas constant.

The estimated stress exponents and activation energies can be used to calculate acceleration factors when the LED package is subjected varying stress conditions.

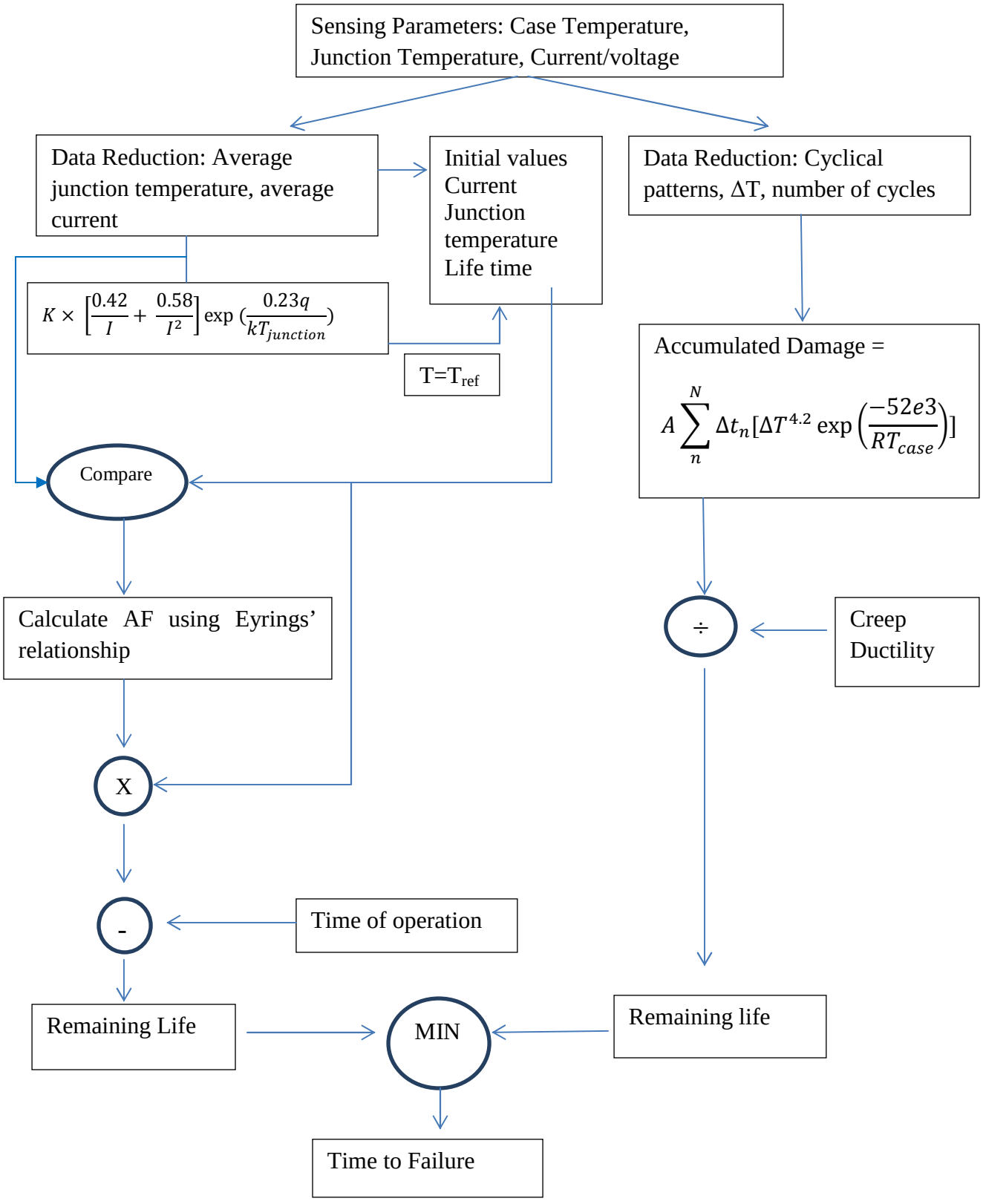


Figure 49. Flow chart for real-time physics based PHM model

4.6 The initial value analysis

These studies establish the utility of series resistance as a reliable contact failure predictor. The above analysis uses rate of change of series resistance rather than a specific absolute value. From the perspective of real-time failure prediction it is the distinct patterns of change rather than the initial values that are important. However, it is extremely useful to know whether there is a relationship between time-to-failure and initial series resistance for quality control. Figure 50 shows that there is no obvious relationship between initial series resistance and time-to-failure. This shows nucleation and growth of voids due to applied stresses are primarily responsible for degradation rather than existing voids or defects in the metallization layer. This observation is consistent with the reported results in a past study [46].

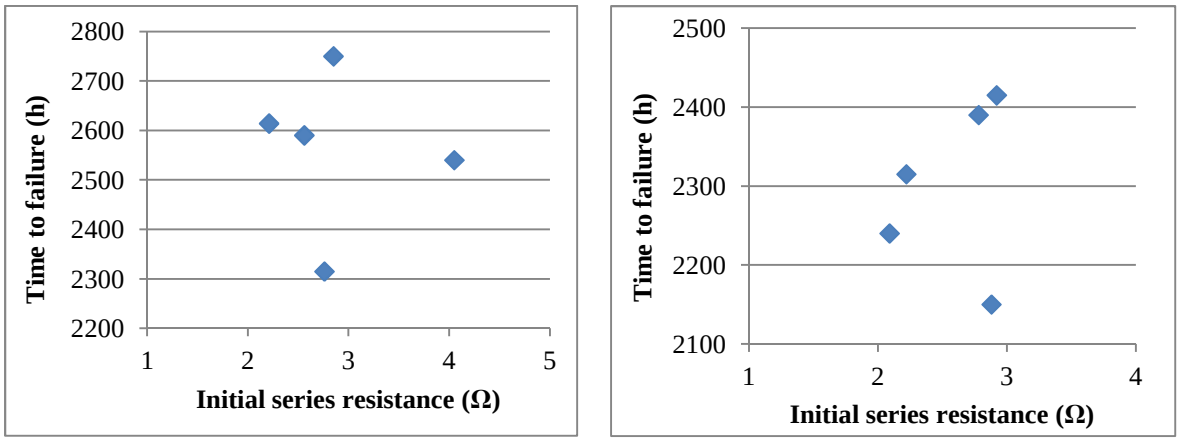


Figure 50. Initial series resistance and time-to-failure at 413K/237A/cm^2 (left), and 423K/237A/cm^2 (right) stress conditions

4.7 Chapter summary

This chapter provides further evidence through post failure analysis and elimination of other possibilities that,

- short circuit failure occurred due to electromigration induced metal diffusion into semiconductor and,
- open circuit failure occurred due to delamination in the submount-substrate interface.

The data driven approach for prognostics and health monitoring based on Euclidean distance (ED) is proposed. The ED combines both series resistance change and thermal resistance change of the LED packages. The calculated ED follows a Gaussian function with time. The ED threshold determination based on different limitation criteria is explained. It is shown that an ED threshold with a negative slope criterion is adequate to capture short circuit failure. The open circuit failure can be detected by using an upper threshold.

A physics based model was derived to estimate life of an LED package for metal migration and delamination failure, at given stress conditions. The metal migration model is a modified Black-Lloyd model for electromigration based on experimental results for metal migration in both metal and semiconductor. The activation energy is determined by the energy barrier for impurity migration along dislocations of GaN. The activation energy in the case of electromigration is determined by the self-diffusion of metal in the metallization layer. In the proposed model void nucleation takes major portion of the life time as oppose to void growth. Relationship for delamination failure with stress conditions was developed using Monkmann-Grant creep failure model. The above two relationships were combined to develop an LED package catastrophic failure model for electrical and thermal contact failures.

5 Conclusions

The dissertation investigated the possibility of developing a reliability prediction methodology by monitoring electrical and thermal parameters of an LED package. An LED package is a sub-system of an LED lighting system, and understanding its behavior under stress conditions is important to assess system reliability. The series resistance and thermal resistance are indicators of health of electrical and thermal contacts of the LED package. Therefore, investigation of long-term behavior of these parameters would shed light on underline failure mechanisms of electrical and thermal contacts. This knowledge is valuable in predicting catastrophic failure, and also in development of LED packages.

There are reliability studies that observed an increase in series resistance and thermal resistance with aging. However, these studies didn't correlate their changes with stress conditions and measured their variation till the point of catastrophic failure. This knowledge is essential in understanding the underline failure mechanism and to develop failure prediction models. There is a significant body of knowledge on degradation kinetics of electrical and thermal contacts in IC packages. However, to what extent that knowledge is transferable for LED packages are not known due to differences in material systems, geometries and stress conditions.

The study investigated the variation of series resistance of LED packages at three different current and junction temperature stress conditions. The series resistance went through four phases, latency period, rapid increase, saturation and sharp decline before failure. The length and nature of these variations changed depending on the stress condition and catastrophic failure mechanism. The void formation in the contact metallization due to electromigration was hypothesized as the underline mechanism for series resistance increase. Theoretical relationship was derived between series resistance change rate and theory of electromigration. This relationship states that series resistance change rate has an exponential dependence on temperature and power law dependence on current density. The experimental data supported the theoretical predictions. The calculated activation energy showed agreement with reported values for Au migration in Au metallization layers in GaAs substrate. The analysis of stress exponents showed that the void growth in the cap layer (Au) is constrained, possibly by the contact layer (Ni), preventing an open circuit failure in ohmic contacts. However, void nucleation process continued throughout the aging process. This mechanism along with Belchs' theory can explain the saturation phase of the series resistance change profile.

The short circuit failure occurred due to formation of metal spikes that creates a junction short-circuit. The metal spike formation was aided by the dislocations in the GaN and electromigration. Theoretical relationship was derived using Ficks' second law of diffusion to explain the series resistance change pattern just before failure. The experimental results agree well with the theoretical model. In addition to series resistance

change profile, ideality factor increase with time, and reverse leakage current increase with time provide supporting evidence that it's the diffusion of metals that caused the short-circuit failure.

There is no known model that could predict failure due to formation of metal spikes under applied stress conditions. The Blacks' electromigration model is an empirical model developed for electromigration in metal contacts. An empirical model was derived using Einstein relationship for diffusion and theory of electromigration.

$$T_{f,die} = K \times \left[\frac{A}{I} + \frac{B}{I^2}\right] \exp\left(\frac{Q}{kT_j}\right)$$

Where, K – LED package specific constant, I – current, k – Boltzman constant, Q – activation energy, T_j – junction temperature, A –parameter that indicates the contribution of void growth in ohmic contact to failure and B – parameter that indicate the contribution of void nucleation

The activation energy was calculated using the samples that showed short-circuit failure at two different temperature conditions. The calculated activation energy of 0.23eV, agrees with the reported activation energies for impurity diffusion in along dislocations in GaN. The parameters, A and B were estimated empirically. The estimated values of 0.42 and 0.58 for A and B suggests that void nucleation phase dominates the failure time. The above empirical model can predict the device life-time when metal diffusion into active region is the dominant failure mechanism for GaN-based LEDs. This is the first time such a model is proposed for LED packages.

The other aspect that was researched in this study is the ability of thermal resistance to predict catastrophic failure in an LED package. The thermal resistance of LED packages increased with aging. Delamination in the die-attach layer was hypothesized as the underline cause of thermal resistance increase. The die-attach layer failure caused a rapid increase in thermal resistance just before failure. At the point of failure LED package temperature reached the melting point of die-attach solder leading to open circuit failure. Delamination is a result of creep strain; therefore, it was hypothesized that thermal resistance change rate is proportional to steady state creep strain rate. A relationship between thermal resistance change rate, temperature and thermo-mechanical stress was developed, based on Dorn-Weeterman power law for creep rate.

$$T_{f,die-attach} = \frac{\epsilon_f}{A \sum_n^N \Delta t_n [\Delta T^n \exp\left(\frac{-Q}{RT_{case}}\right)]}$$

Where, ϵ_f – creep ductility, ΔT- temperature difference between junction and case, Q – activation energy, T_{case} – case temperature, A – LED package specific constant, R –

universal gas constant, Δt_n – time spent at a given stress condition and N – number of cycles

The activation energy and stress exponent was calculated using measured thermal resistance change rates at different temperature and current stress conditions. The measured activation energy of 52kJ/mol and stress exponent of 4.2 compares well with the reported values for Sn-Ag-Cu solder, the die-attach solder used at submount-substrate interface. The results showed that dislocation creep is responsible for creep induced plastic deformation. Physics based time to failure model was proposed for the first time to predict catastrophic failure of LED packages, when creep induced thermal interface delamination is the dominant failure mechanism.

The findings of this dissertation have implications in failure prediction for GaN-based LEDs and for reliable LED package design. The goal of this dissertation is to develop a prognostics and health monitoring (PHM) scheme for LED packages. A scheme to implement PHM is proposed based on the experimental observations. The two schemes, one based on data driven approach and the other based on physics of failure approach is presented. The Euclidean distance (ED) vector that considers both series resistance and thermal resistance change was calculated as a function of time. The ED vector magnitude change with time showed strong correlation to a Gaussian function for LED packages that showed short-circuit failure. The short-circuit failure could be predicted by setting an ED threshold with a negative slope detection criterion. The ways to improve detection accuracy and threshold determination is discussed. The open circuit failure can be detected by setting an upper threshold.

Physics of failure model was developed assuming that metal diffusion into semiconductor and delamination at die-attach as two independent failure mechanisms. This combined model could be used to predict the LED package life time based on catastrophic failure. As an example let us assume that the base case operating conditions were $T_j = 150^0$C, I = 1A and $T_{case} = 95^0$C. If there is a 10% increase in T_j due to an increase in ambient temperature, then according to the model the LED package life would decrease by 30%, and it would be an open circuit failure due to die-attach delamination. If the current is increased by 10% and taking into account of changes in temperatures caused by current, the model predicts a 30% reduction in LED package life. However, in this case it would be a short-circuit failure due to metal diffusion.

The same model can be used to predict catastrophic failure of an LED package in a PHM scheme. In this case the life prediction can be modified according to changes in the in-situ stress conditions. A flow chart for a real-time physics of failure based remaining useful life estimation model is also presented. This is the first known study that developed a catastrophic life estimation model based on electrical and thermal contact failure in LED packages.

The findings of this dissertation is also helpful in developing reliable LED packages, especially the high density, high current and high operating temperature package development. LED package designer could use the physics based model to predict the failure of the die or thermal interface at the targeted current or temperature condition. He has to adjust the model parameters based as they are specific to materials and geometry. Approach to calculate those model parameters are described in great detail in this study. From the contact metallization layer design point of view it is useful to estimate the activation energy for vacancy diffusion using the series resistance slope analysis presented in section 2.7.4. A reliable contact metallization design should have large activation energy. Further the current exponent analysis given in appendix c is useful to determine whether void growth or void nucleation mechanisms dominate during aging. From the perspective of LED package reliability contact metallization design should reduce void growth phase.

The diffusion of Au along dislocations of GaN is a reliability concern for many GaN-based device applications. This phenomenon was reported in previous InGaN based LED and GaN-based HFET reliability studies. This dissertation calculated the activation energy for this diffusion process and proposed a method to estimate diffusion coefficient of Au in GaN-based semiconductor. A more thorough understanding of diffusion of impurities along dislocations in GaN is required to validate these experimental observations. Further theoretical and experimental analysis is required to establish whether reduction of defect density in GaN would have a significant impact on metal diffusion.

The dissertation also showed that in terms of die-attach failure that creep deformation is the dominant failure mechanism. Simple analyses of homologues temperatures are sufficient to establish this fact. However, the interesting empirical observation in this study is that dislocation creep is the dominant failure mechanism. This information is useful for die-attach material designers to investigate the possibility of reducing dislocation creep without significantly increasing the melting point.

5.1 Future studies

The proposed future studies could address the limitations of the proposed model explained in section 4.5. The proposed model needs to be validated at different stress conditions, and using different LED package types. The findings of the dissertation could be used to design such experiment, possibly with a larger population. It would be particularly useful to know whether there is a threshold temperature or current stress condition below which the failure mechanisms discussed in this study would be

insignificant. Thresholds have been determined for IC packages, but such a study is yet to be performed for LED packages.

The LED package type used in this study has a vertical die-structure. While this is the LED package type widely used in the semiconductor industry, flip-chip packages are also being used in many lighting applications. A pilot test was done using a flip-chip LED package and these packages also showed a significant increase in series resistance with aging. A comprehensive study with a similar experimental design as discussed in this study using flip-chip LED packages can be used to verify the validity of the above model.

In this model the two stress conditions used was current and temperature. The impact of other stress conditions on catastrophic failure of LED packages must be investigated. Application point of view, it is useful to know the impact of stresses due to vibration on contact failure. Vibration depending on the amplitude and frequency induce fatigue in contacts, and may accelerate their failure. The proposed model can be refined by incorporating the impact of vibration on failure time.

There is no-known theoretical model that attempts to model metal migration along dislocations in GaN. Theoretical model that could explain this complex phenomenon and possibly the experimental observations is extremely useful. Theoretical analysis that could explain the model would not only makes it stronger but also provides an insight into failure mechanism.

5.2 New knowledge contribution

This dissertation discusses two dominant failure mechanisms that degrade electrical and thermal contacts of LED packages and cause catastrophic failure. These mechanisms were metal diffusion into active region and creep deformation at die-attach solder layers. The variation of LED package series resistance and thermal resistance until the point of catastrophic failure of LED package was investigated. The analysis of these parameters just before failure shed knew knowledge on underline failure mechanism. The analysis also presented the possibility of using these parameters as early predictors of catastrophic failure of an LED package for the first time. The dissertation also presents the influence of current and temperature stress conditions on these parameter changes. The physics that governs such changes are explained for the first time for GaN-based LED packages. All these analyses were synthesized to develop an empirical model to predict catastrophic failure. This is the first known model that could predict catastrophic failure of LED packages based on electrical and thermal contact failure.

6 References

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Appendix A: Ohmic contact formation in GaN

The Schottky-Mott theory, explain the formation of Schottky Barrier Height (SBH) when a metal and semiconductor is in contact [33], [161]. This is a potential barrier that electrons have to overcome when moving across the metal-semiconductor interface. The Schottky-Mott theory states, that when a metal and semiconductor forms a contact, charges redistribute across the contact so that at point of stability, Fermi levels becomes equal. According to the theory, changes in SBH are equal to changes in the metal work function. The experimental evidence has shown that this is not the case for all semiconductor materials. However, in the case of GaN, SBH is dependent on the work function of the contact metal [162], [163].

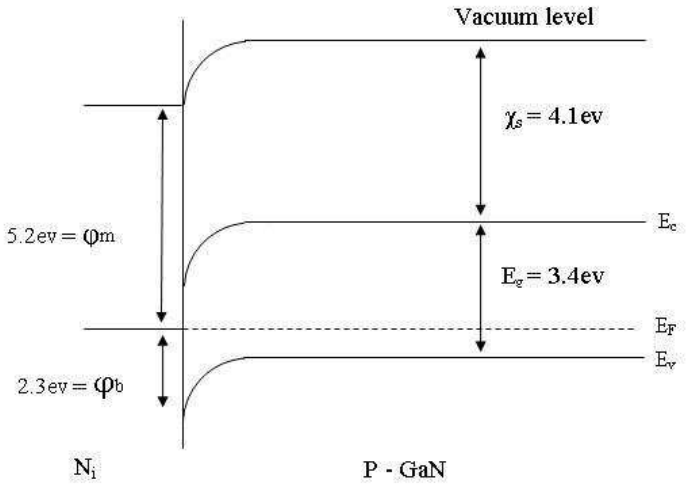

Figure 51. Band diagram of Ni contact on P-GaN

$$q\varphi_b = \varphi_m - X_s$$

φ_b – barrier height, φ_m – metal work function, X_s – electron affinity

The above equation can be used to select a suitable metal for ohmic contact formation for n-GaN. The measured electron affinity (X_s) of GaN is 4.1eV[164]. Therefore, any metal with a work function less than 4.1eV will form an ohmic contact with n-type GaN [165], [166]. The potential barrier height (φ_b) depends on the metal work function (φ_m) as described in the above equation. There are a variety of metals that meet the above criterion; therefore, formation of n-GaN ohmic contact is not a significant challenge for GaN-based LEDs. However, there are significant challenges in forming n-type ohmic contacts N-face GaN, used in vertical structure LEDs [167], [168].

Formation of ohmic contact to p-GaN is challenging since ideally the work function of the metal should be greater than 7.5eV (electron affinity (X_s) – 4.1eV + Band gap (E_g) – 3.4eV). There are no metals that have such large work functions. However, industry has used Ni/Au metal alloys to form ohmic contacts on P-GaN [169]. Energy band diagram for the Ni/P-GaN interface is shown in Figure 51. The Ni/Au contact has a bi-metal structure where Ni acts as the contact layer, and Au acts as the cap layer.

Even in the case of Ni/p-GaN contact, carriers have to overcome a significant potential barrier of 2.3eV. A common strategy adopted to lower the barrier is to form an intermediate semiconductor layer that is heavily doped. However, achieving high dopant concentrations in P-GaN has proven to be challenging due to the formation of stable Mg-H complexes [170]. The material interactions that occur between P-GaN and Ni/Au metal system is analyzed, to understand the ohmic contact formation process and fabrication parameters that affect the contact resistance [171], [33], [173], [174], [175], [176], [177]. These studies highlight the importance of inter-diffusion of Au and Ga through the Ni contact layer in formation of ohmic contact. However, this could pose a long-term reliability issue if Au atoms diffuse into active region of the semiconductor via the vacancies created by the out-diffused Ga.

The addition of different metal barriers (ex: Ti, W_2B, CrB_2, etc..) are suggested as a remedy to prevent out-diffusion [178]. In addition many different material combinations (ex: Pd, Pt, Ru, Re, etc.) with high work functions were studied to form low resistance ohmic contacts for p-type GaN [178]. However, the Ni/Au scheme still remains the popular choice in the LED industry. Another disadvantage of Au/Ni metal contact is its poor optical transmission and low refractive index. The poor optical properties would mean that thin metallization layers with high current densities are used in LED packages increasing the susceptibility for failure mechanisms such as electromigration. Several strategies have been investigated in past studies to improve optical properties of ohmic contacts [179], [180], [181], [182], [183], [184], [185].

In flip-chip packages light is extracted via the transparent sapphire substrate. Therefore, in this package type reflective ohmic contacts are desired. In flip-chip packages metals such as Ag, Al, and Rh are the preferred choice, due to their high reflectance properties. In these packages Ag is widely used as the ohmic contact, and low contact resistivity of Ag contact is attributed to formation of Ag-Ga compounds during the annealing process. The Ga vacancies in the p-GaN layer act as acceptors reducing the contact resistance of Ag/p-GaN interface [186], [187]. However, at high temperatures reflectivity of Ag decreases and resistance increase due to formation of interfacial voids that reduces the contact area [186].

Appendix B: Series resistance data

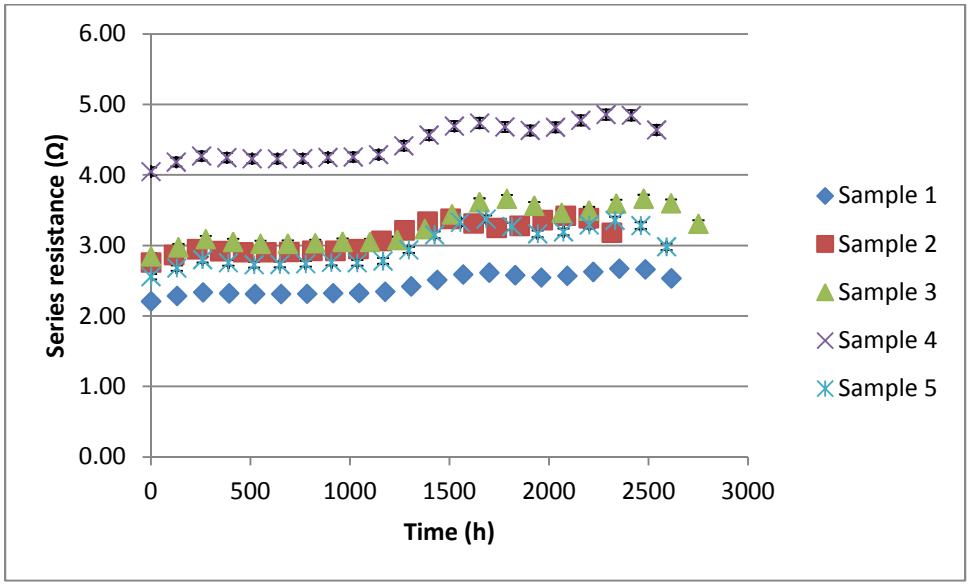

Figure 52. Series resistance change with time at 413K and 237A/cm^2 current density

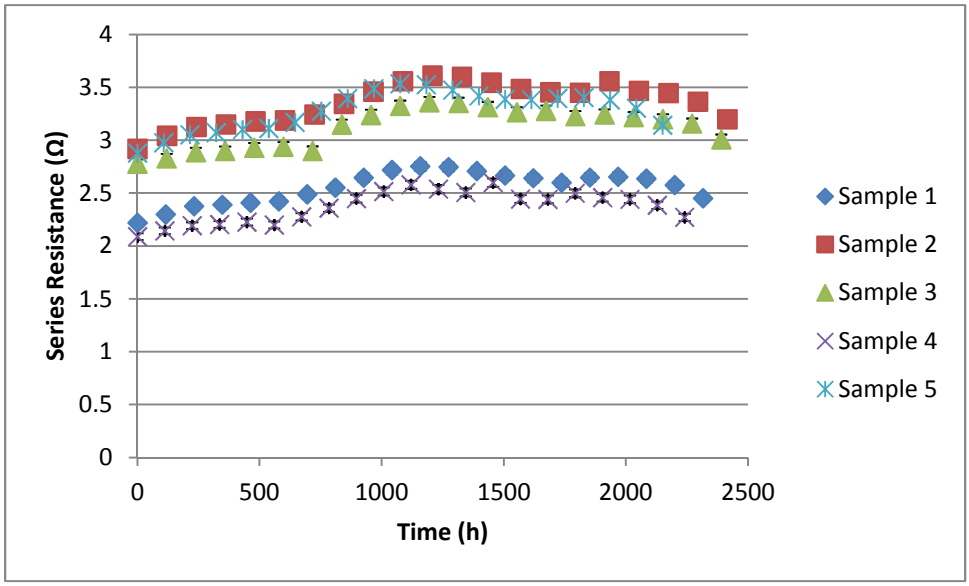

Figure 53. Series resistance change with time at 423K and 237A/cm^2 current density

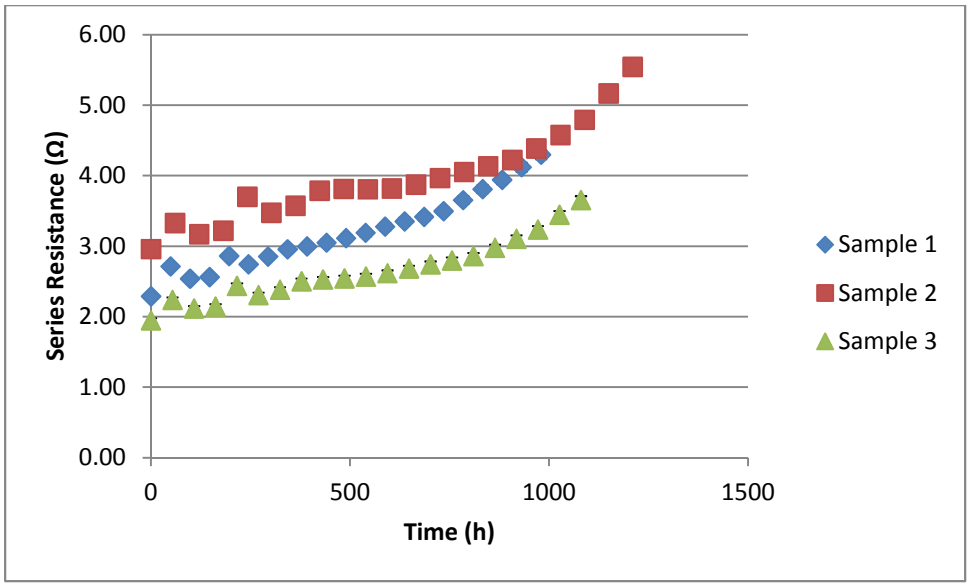

Figure 54. Series resistance change with time at 448K and 237A/cm^2 current density

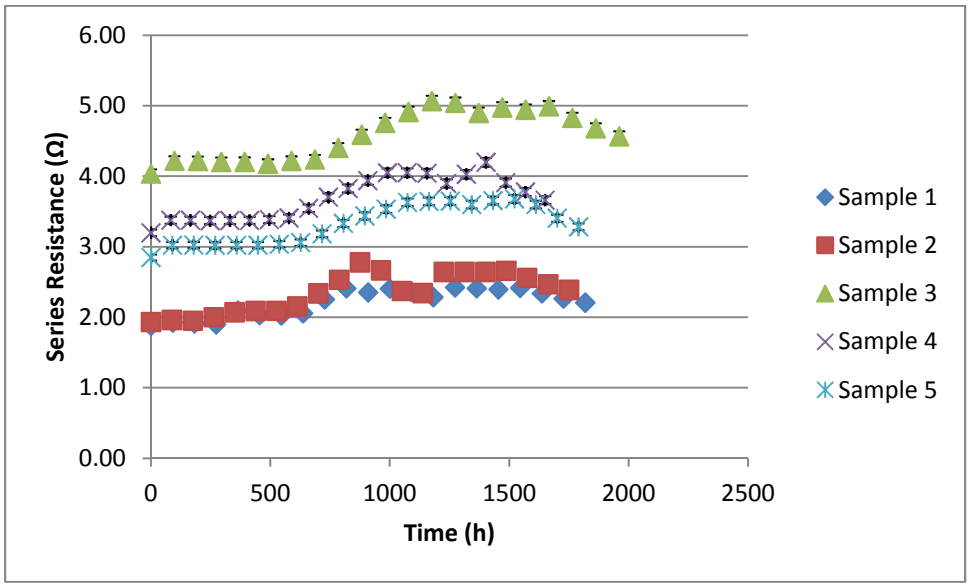

Figure 55. Series resistance change with time at 423K and 296A/cm^2 current density

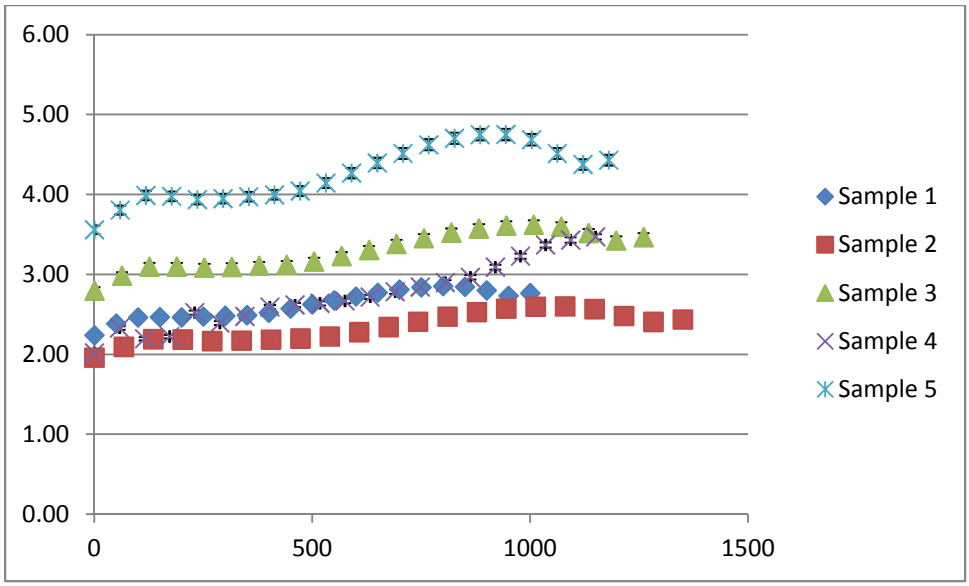

Figure 56. Series resistance change with time at 423K and 355A/cm^2

Appendix C: Recent developments in electromigration life-time models

The most of recent work on electromigration induce failure in IC packages focus on separating the two phases [115], [188]. The activation energy for both phases is the same, since the vacancy migration mechanism is the same. The activation energy calculated using the Arrhenius model may not reflect the true activation energy, because there are other temperature dependencies those effects the failure time. As an example the void nucleation process in a material requires a threshold stress, which may be provided through a combination of electromigration stress (Arrhenius model) and thermo-mechanical stress. A complex model which addresses these issues was presented by Lloyd R. in 2007 [115].

$$MTF = [\frac{AkT}{j} + \frac{B(T)}{j^2}]\exp(\frac{Q}{kT})$$

Where, A and B are constants that include geometric information

The constant, B has temperature dependence, and all other terms have usual meaning as explained in previous equations. At constant temperature conditions, the above model was used to fit the experimental data. The ratio of the two constants would indicate the relative duration of the void nucleation and void growth. As per the results in Figure 57, approximately 37% of the time is spent on void nucleation phase. As expected the void growth phase dominates up to phase 2; this is the region that shows the largest increase in series resistance.

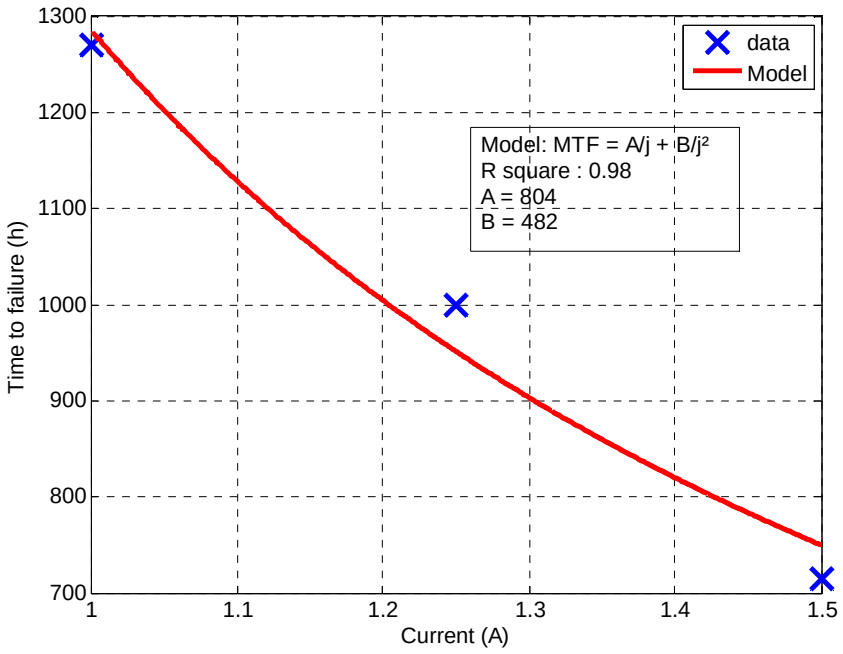

Figure 57. Lloyd model fit to experimental data

The activation energy can be re-calculated considering the additional temperature dependencies indicated in the above equation. In practical applications the metallization layer is in contact with another metal/semiconductor and a dielectric layer. The thermal expansion coefficient mismatch induces a stress on the metallization layer in addition to electromigration stress. This thermo-mechanical stress facilitates void nucleation. This is a temperature dependent mechanism, and several models incorporated this into the electromigration model. Incorporation of these stress effects would increase the calculated activation energy as shown in Table 9.

Table 9. Activation energy for electromigration using different models

Model	Activation energy (eV)
Blacks' model	0.46
Void growth only model	0.49
Korhonen's model: B(T) $\propto T^2$[114]	0.53
Clement's model: B(T) $\propto T^3$ [189]	0.57

Appendix D: Thermal resistance measurement for DC LED

The equation used for thermal resistance calculation of LED packages is [10],

$$R_{\theta J-X} = \frac{T_j - T_x}{P_H}.$$

Where, T_j - junction temperature, T_x – reference temperature, and P_H – thermal power dissipation

The above thermal resistance is also referred to as residual thermal resistance. The measured thermal resistance in the context of this study is,

$$R_{\theta J-C} = \frac{(T_j - T_c)}{P_e}.$$

Where, $R_{\theta J\text{-}C}$ – measured thermal resistance, T_j – junction temperature, T_c – case temperature, and P_e – electrical input power

The reference temperature, T_x of an LED package is typically its case temperature. The heat flow lines are perpendicular to the isothermal surfaces. The thermal flux lines are parallel to the heat flow lines. Thermal flux network and isothermal surfaces are linked to one another, where one is required to define the other. The measured thermal resistance using the above equation is specific to the isothermal surface and therefore to the heat flux network. Therefore, any change in heat flux network will change the measured thermal resistance[125]. Thermal resistivity is a material specific metric which is calculated as,

$$r = \frac{(T_1 - T_2)}{q \times x}.$$

Where T_1, T_2 are temperatures of two isothermal surfaces separated by a uniform material, x – thickness of the material, and q – heat flux per unit area

The thermal power dissipated in the thermal path is dependent on the quantum efficiency of the device; therefore, it is dependent on series resistance [190]. This thermal resistance value combines the contributions of different materials and interfaces in the thermal conduction path towards final thermal resistance. These contributions could be separated using transient thermal analysis.

The junction temperature of an LED package cannot be measured directly. This is because, junction is by definition is the location at which electrons and holes recombine. This is not a physical location that could be accessed using an intrusive thermal measurement technique. Therefore, semiconductor industry uses indirect junction temperature estimation techniques. These methods use forward voltage as the

temperature sensitive parameter. The theoretical relationship between forward voltage of a diode and its junction temperature is established using the following equation.

$$\frac{dV}{dT} = \frac{V}{T} - \frac{(V_{Go}+mnV_T)}{T}, V_T = \frac{kT}{q}$$

Where, V- voltage, T- temperature, k- Boltzman constant, q-electron charge, V_{Go}, m, and n – device specific constants

The measured forward voltage of the diode has a linear dependence on junction temperature. The goal is to measure forward voltage at a known junction temperature. This is achieved by applying a small current that is,

- Adequate to forward bias the LED, and
- Not large enough to cause joule heating in the junction.

The chosen calibration current for this study is 1mA. It is assumed that at this current junction temperature is equivalent to controlled ambient temperature, since heat generation in the junction is negligible. The controlled ambient temperature in this study is the cold plate temperature of the thermo-electric cooler. The case temperature measurement point is a location next to the ceramic substrate. The case temperature is measured using a T-type thermocouple that was attached using solder. The LED package is attached to the thermoelectric cooler using mechanical screws. The calibration is performed by varying the cold plate temperature from 25^0C to 75^0C in 5^0C increments. The voltage is measured after LED reached thermal stability at each temperature setting. The thermal stability was defined as the point at which the variation of five consecutive case temperatures measured at every 1min interval is less than 0.1^0C. The calibration factor (K) is calculated from measurement results,

$$\text{K = gradient of calibration curve} = \frac{(V_{T1} - V_{T2})}{(T_1 - T_2)}$$

Where, T_1 and T_2 are two temperatures and V_{T1} and V_{T2} are two forward voltages at those two temperatures.

After calibration the LED is powered using its heating current (I_H) and allowed to thermally stabilize at a controlled ambient temperature. The measurement procedure is illustrated in the Figure 58. As indicated prior to measurement the calibration current (I_M) is applied and voltage (V_{Ff}) is measured at the controlled ambient temperature. Then the heating current (I_H) is applied and the system is allowed to thermally stabilized at the same ambient temperature. As indicated in Figure 58, the forward voltage, V_H of the diode decrease with time due to junction heating. When LED package reach thermal stability V_H is measured for electrical input power calculation. Then the current is switched from I_H to I_M and voltage of the diode is measured after a short measurement

delay (t_{MD}). The measurement delay is determined by the switching speed, and pulse jitter of the measurement system. The measurement delay was fixed at 100μs. The voltage would have an instantaneous response to current change and would decrease up to V_{Fi}. This is the voltage that corresponds to a heated junction at the calibration current. The temperature rise in the junction due to I_H, can be calculated as,

$$\Delta T_j = \frac{(V_{Fi} - V_{Ff})}{K}.$$

The absolute junction temperature (T_j) is calculated as,

$$T_j = \Delta T_j + T_a \ .$$

Where, T_a – ambient temperature

The junction-to-case thermal resistance ($R_{\theta J\text{-}C}$) can be calculated as,

$$R_{\theta J-C} = \frac{(T_j - T_{case})}{V_H \times I_H} \ .$$

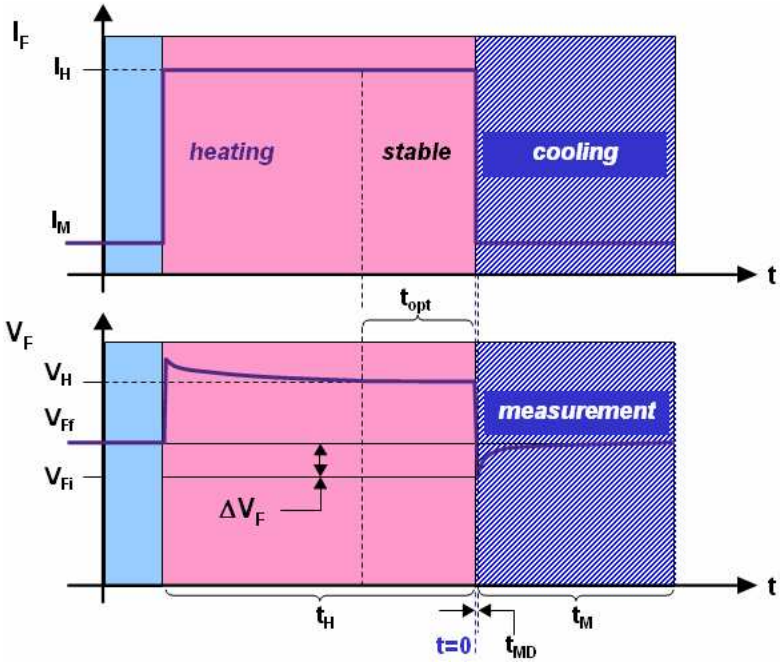

Figure 58. The measurement procedure [191]

Transient thermal analysis

Thermal resistance is measured at steady state; therefore, thermal capacitance of the thermal path is not reflected in the metric. Thermal impedance on the other hand captures the effects of both thermal resistance and thermal capacitance in the metric. Thermal impedance is a time dependent quantity.

$$R_{\theta J-X}(t) = Z_{\theta J-X} = \frac{\Delta T_j(t)}{\Delta P_H}$$

Where, $Z_{\theta j\text{-}x}$ – thermal impedance between two isothermal surfaces, J and X, ΔT_j (t) – difference in junction temperature at two time intervals, ΔP_H – difference in thermal power dissipation in the junction.

In transient thermal analysis the device is modeled as either a Cauer or a foster network with thermal resistive and capacitive elements [192], [193], [194], [195], [196]. Even though, the foster network representation simplifies the analysis, only the Cauer network representation has physical meaning. A realistic Cauer network model for LED packages is given in Figure 59. However, to simplify the analysis and to link extracted parameters with the thermal interfaces of the package, it is assumed that contribution of material layers on top of the die is negligible [193]. Further, one dimensional heat transfer is assumed.

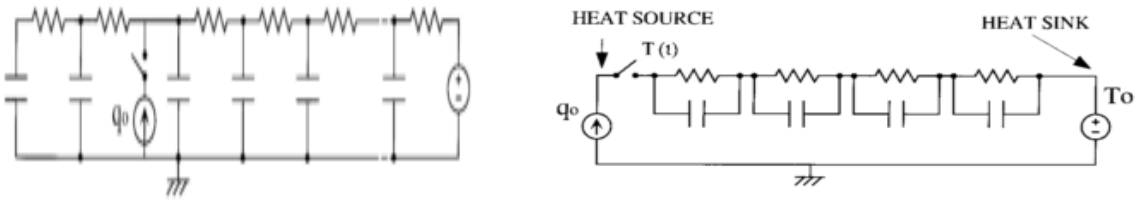

Figure 59. The Cauer thermal network (left) and foster thermal network (right) models for LED package [193]

The transient response for the above network could be stated as [194],

$$f(t) = \sum_{i=0}^{\infty} T_i \left[1 - e^{\frac{-t}{\tau_i}}\right].$$

Where, τ_i – time constant for the i^{th} segment, t – time and T_i – amplitude factor

If foster network representation is assumed; then R_i- thermal resistance, and C_i-capacitance for each element can be computed as,

$$R_i = \frac{T_i}{P_{in}}$$

$$C_i = \frac{\tau_i}{R_i}$$

Where, P_{in} – thermal power dissipated

The differential structure function, constructed using thermal transient analysis of LED packages with different degrees of delamination is shown in Figure 60. It was assumed the package could be represented as the Cauer network that has a continuous time constant spectrum[195]. The figure plots the parameter K, which is the derivative of cumulative thermal capacitance with respect to cumulative thermal resistance. The physical parameters embedded in K are [195],

$$K(R_\theta) = C_v \gamma A^2$$

Where, C_v – volumetric heat capacitance, γ – thermal conductivity and A – cross-sectional area of the heat flow

Therefore, differential structure function plots variation of thermal resistance with the above mentioned parameters of a package.

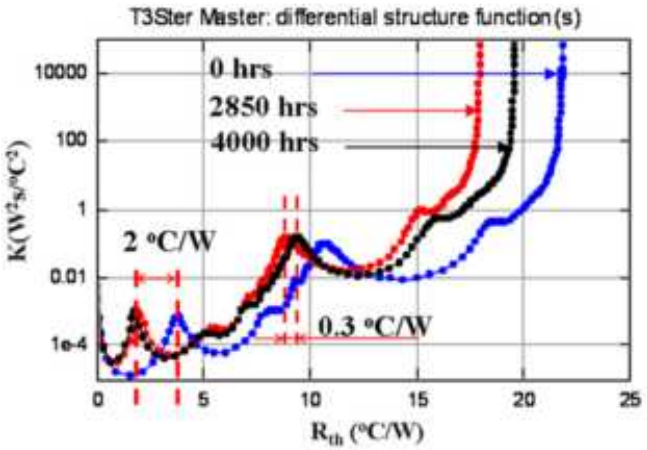

Figure 60. Differential structure functions of an LED package subjected to aging [98]

Appendix E: Creep deformation

Creep is an irreversible structural deformation process a material undergoes when subjected to stress. Creep response of a material can be divided into three stages, primary, secondary, and tertiary. The variation of creep strain with time is given in Figure 61, at different temperature and applied stress conditions. The curve B is when the temperature is low; curve C, is when temperature and stress is highest; curve A, is at moderate temperature and stress conditions. The mechanism for primary or transient creep is not very well understood, but it is stated that transient response makes structural deformation difficult. Therefore, creep strain rate reduces as a function of time [197]. At secondary creep stage, material is subjected to steady creep strain. At tertiary stage the material will undergo rapid deformation leading to its fracture [198], [199].

Almost all known mechanisms of creep depends on diffusion and therefore, on temperature. The concept of homologous temperature plays an important part in determining the creep deformation of a material. The homologous temperature is calculated as,

$$T_H = \frac{T}{T_M} \ .$$

Where, T_H – homologous temperature; T_M – melting point

If $T_H > 0.5$, diffusion dominates in the operating temperature; therefore, the material is subjected to creep strain. The Dorn-Weerteman power law states that [141],

$$\acute{\varepsilon} = A\sigma^n e^{-(\frac{Q}{RT})}.$$

where, έ – creep strain rate; σ – stress; n – stress exponent; q-activation energy; R – universal gas constant; T – temperature

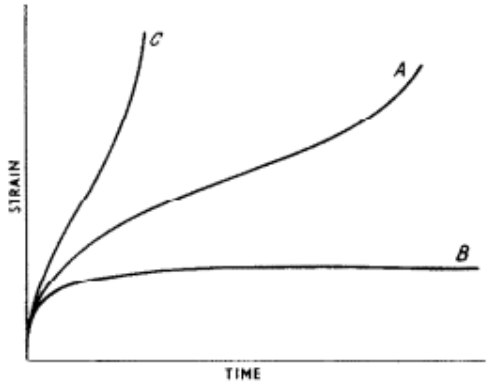

Figure 61. Creep curves [197]

Appendix F: Thermal resistance data

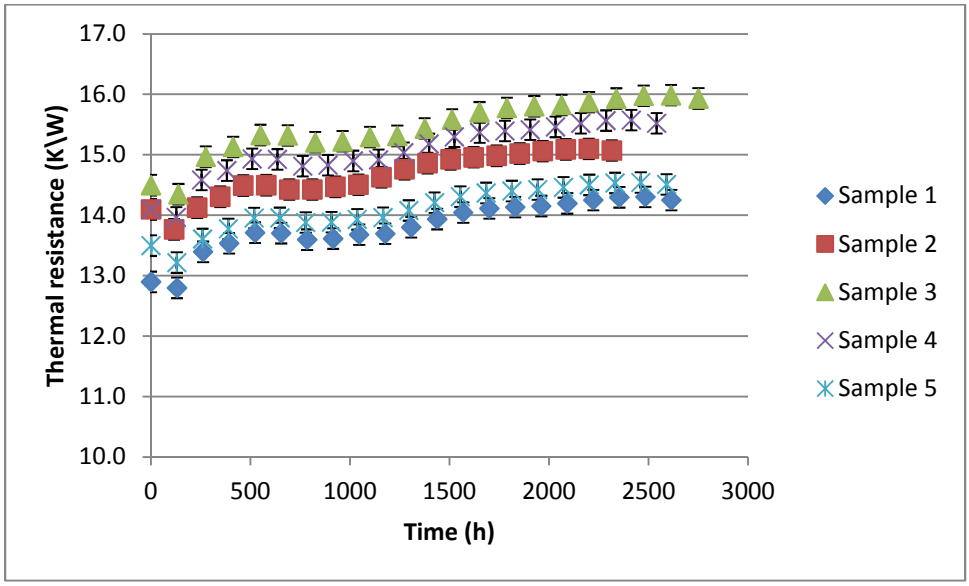

Figure 62. Thermal resistance change with time 413K and 237A/cm^2 current density

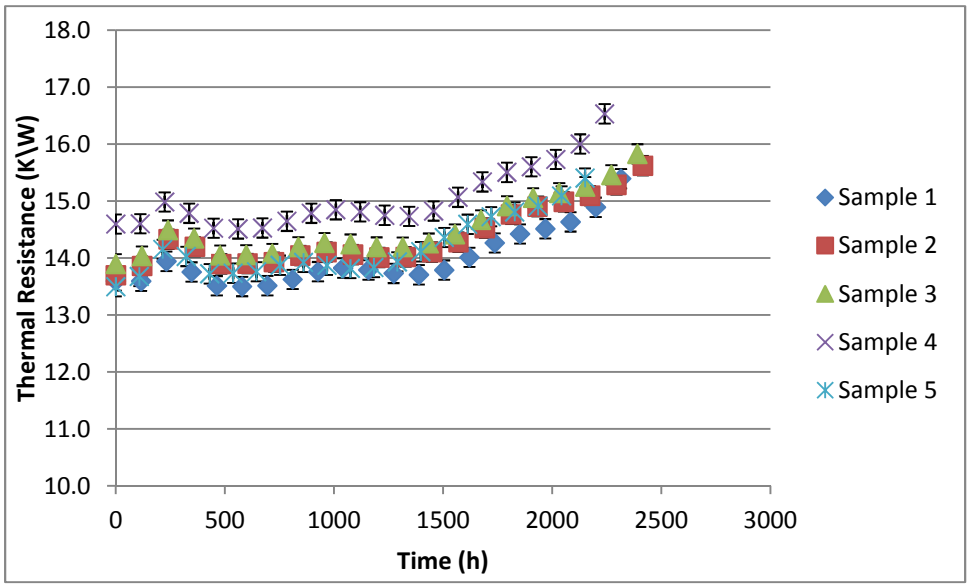

Figure 63. Thermal resistance change with time 423K and 237A/cm^2 current density

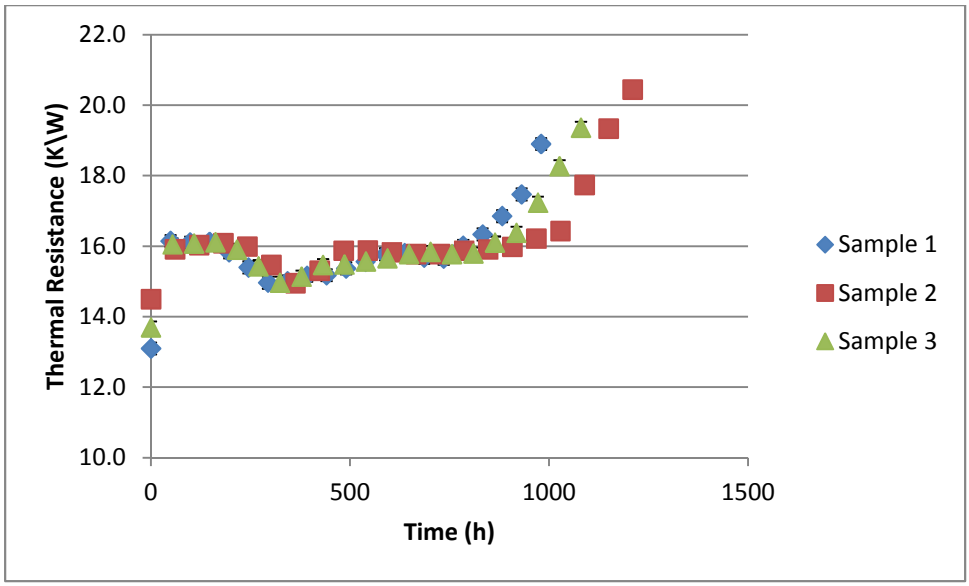

Figure 64. Thermal resistance change with time 448K and 237A/cm^2 current density

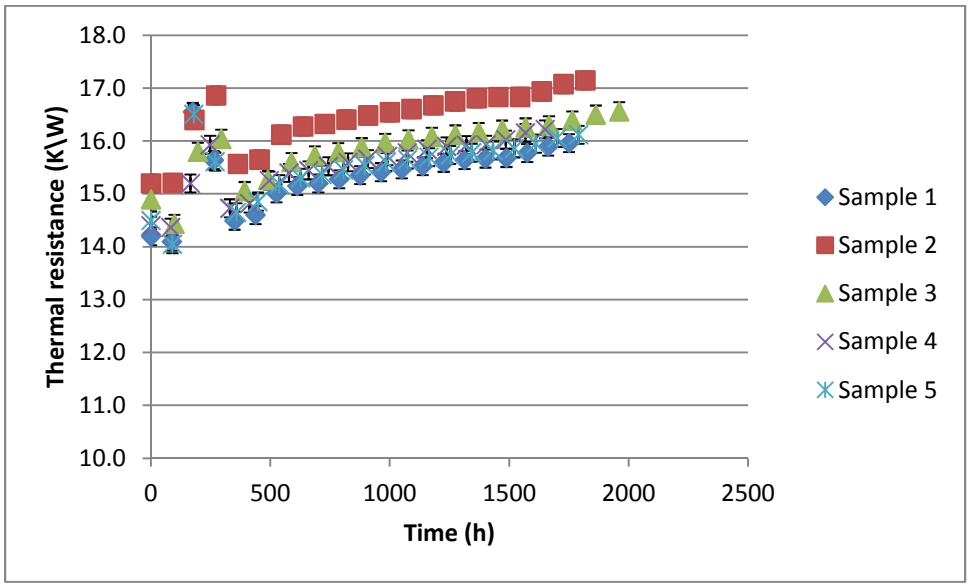

Figure 65. Thermal resistance change with time 423K and 296A/cm^2 current density

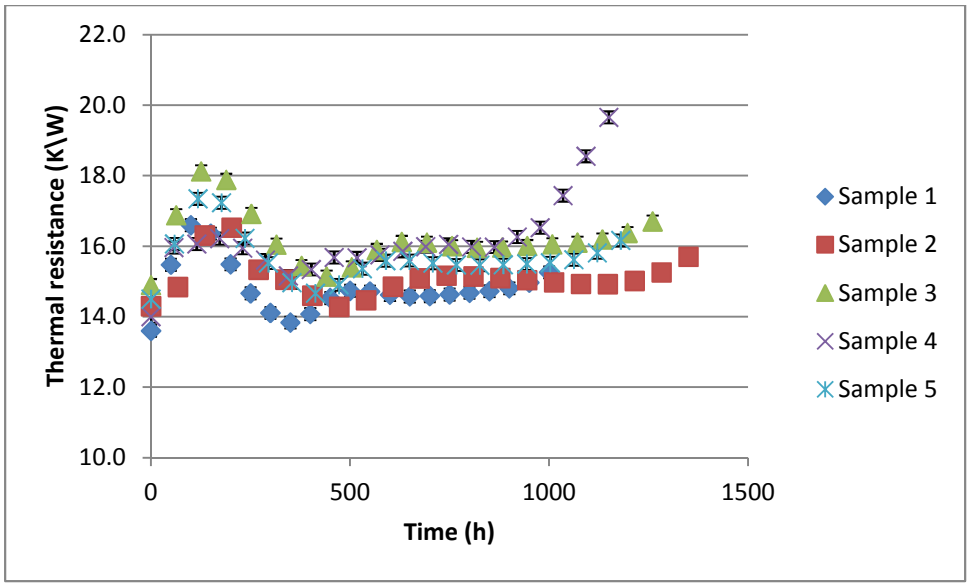

Figure 66. Thermal resistance change with time 423K and 355A/cm^2 current density

Appendix G: Uncertainty analysis

The measurement uncertainty of the measurement set-up is calculated using the propagation of error formula [200]. The standard deviation of a two variable function of the form $Y = AX + BZ$ is given by,

$$S = \frac{1}{\sqrt{N}} \sqrt{(A^2 S_x^2 + B^2 S_z^2)}$$

Where, N – number of repeated measures, S_x and S_y are standard deviation of two variables X and Y

The standard deviation for a two variable function of the form,

$Y = \frac{X}{Z}$, is given by,

$$S = \frac{1}{\sqrt{N}} \times \frac{X}{Z} \times \sqrt{(\frac{S_x^2}{X^2} + \frac{S_Z^2}{Z^2})}$$

Where, all terms have the meaning mentioned above.

The 95% confidence band was considered as the standard deviation for parameters extracted from figures. The uncertainty of different measurement parameters are given in Table 10.

Table 10. Uncertainty of measurements

Parameter	Uncertainty
Calibration factor (K)	±3% (based on 95% confidence interval)
Voltage	±0.002 (based on 100 repeated measures)
Temperature	$\pm 1^0$C (Standard error for T-type thermocouple)
Junction temperature	$\pm 1.2^0$C (Calculated)
Thermal resistance	±0.17K/W (Calculated)
Normalized thermal resistance	±0.01(Calculated based on 3 repeated measurements)
Series resistance	±1.5% (based on 95% confidence interval)
Normalized resistance	±0.02 (Calculated based on 3 repeated measurements)

The uncertainty of physics based life-time estimation model is assessed using propagation of error formulas. If R = R(x, y), then the uncertainty of R can be obtained by,

$$\delta R = \sqrt{(\frac{\partial R}{\partial x}\delta x)^2} + (\frac{\partial R}{\partial y}\delta y)^2$$

The life-time prediction model for die failure is given by,

$$T_{f,die} = K \times \left[\frac{A}{I} + \frac{B}{I^2}\right] \exp\left(\frac{Qq}{kT_{junction}}\right)$$

$$\frac{\partial T_f}{\partial A} = \frac{1}{I} \exp\left(\frac{Qq}{kT}\right)$$

$$\frac{\partial T_f}{\partial B} = \frac{1}{I^2} \exp\left(\frac{Qq}{kT}\right)$$

$$\frac{\partial T_f}{\partial Q} = \left(\frac{A}{I} + \frac{B}{I^2}\right) \exp\left(\frac{Qq}{kT}\right) \times \frac{q}{kT}$$

$$\frac{\partial T_f}{\partial Q} \gg \frac{\partial T_f}{\partial A}, \frac{\partial T_f}{\partial B}$$

$$\delta T_f = K \times \frac{\partial T_f}{\partial Q} \times \delta Q$$

The base case was chosen as the time to failure at 1A current and 423K junction temperature. The uncertainty of activation energy is ±0.025eV. The uncertainty was determined considering that reported values of activation energy for impurity migration along dislocations in GaN range from 0.23eV-0.28eV. This gives a prediction uncertainty of ±110h for die failure time.

$$T_{f,die-attach} = \frac{2.7}{A \times [\Delta T^n \exp\left(\frac{-Q}{kT}\right)]}$$

$$\frac{\partial T_f}{\partial n} = \left(\frac{1}{\Delta T}\right)^n \ln\left(\frac{1}{\Delta T}\right) \times 2.7 \exp\left(\frac{Q}{RT}\right)$$

$$\frac{\partial T_f}{\partial Q} = \frac{2.7}{\Delta T^n} \exp\left(\frac{Q}{RT}\right) \times \frac{1}{RT}$$

$$\frac{\partial T_f}{\partial Q} \ll \frac{\partial \mathrm{T_f}}{\partial \mathrm{n}}$$

Therefore, $\delta T_f = \frac{1}{A} \times \frac{\partial T_f}{\partial n} \times \delta n$

The same base case as above was chosen, and uncertainty of the exponent is ±0.4. The error was determined using the 95% confidence band for the exponent. Previous studies reported an exponent of 4, whereas the measured exponent in this study is 4.2. This gives a prediction uncertainty of ±255h.

Appendix H: Thermo-mechanical stress calculation

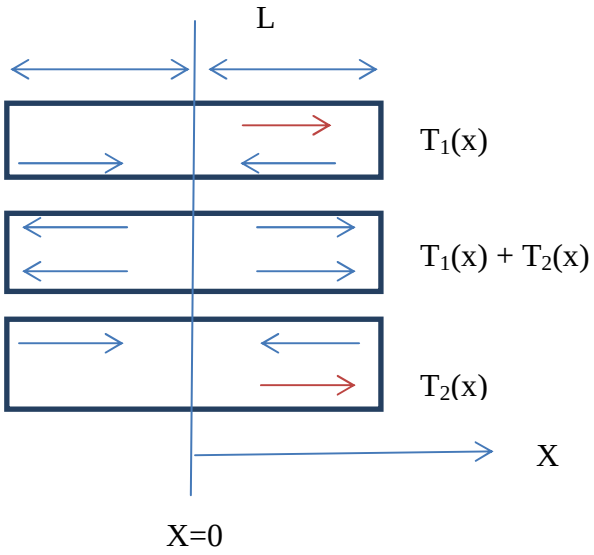

Figure 67. Stress diagram for a tri-material system

The shearing forces created in the interfaces of a tri-material assembly when they are heat up by ΔT are indicated in the figure above. In addition to the shearing force there is a bending moment on each material, direction of which is determined by the right hand rule. These forces along with unrestrained thermal expansion would cause longitudinal displacements, d(x) at each interface. If the tri-material assembly is to maintain its integrity these displacements should be in equilibrium.

The sign convention:

All compressive forces and displacements are (-) ve

All tensile forces and displacements are (+) ve

For equilibrium,

$$-d_1(x) = d_{21}(x)\ ;\ d_{23}(x) = -d_3(x)$$

$$-d_1(x) = \alpha_1 \Delta t x - \lambda_1 \int_0^x T_1(\in) d \in + \beta_1 \tau_1(x) - \frac{h_1}{2} \int_0^x \frac{d\epsilon}{\rho(\epsilon)}$$

$$d_{21}(x) = \alpha_2 \Delta t x + \lambda_2 \int_0^x T_1(\in) + T_2(\in) d \in - \beta_2 \tau_1(x) + \frac{h_2}{2} \int_0^x \frac{d\epsilon}{\rho(\epsilon)}$$

$$d_{23}(x) = \alpha_2 \Delta t x + \lambda_2 \int_0^x T_1(\in) + T_2(\in) d \in - \beta_2 \tau_2(x) + \frac{h_2}{2} \int_0^x \frac{d\epsilon}{\rho(\epsilon)}$$

$$-d_3(x) = \alpha_3 \Delta t x - \lambda_3 \int_0^x T_2(\in) d \in + \beta_3 \tau_2(x) - \frac{h_3}{2} \int_0^x \frac{d\epsilon}{\rho(\epsilon)}$$

This would lead to following set of equations,

$$(\alpha_2 - \alpha_1)\Delta t x = -(\lambda_1 + \lambda_2) \int_0^x T_1(\in) d \in -\lambda_2 \int_0^x T_2(\in) d \in + (\beta_2 + \beta_1)\tau_1(x) - \frac{(h_1 + h_2)}{2} \int_0^x \frac{d\epsilon}{\rho(\epsilon)}$$

$$(\alpha_3 - \alpha_2)\Delta t x = -(\lambda_3 + \lambda_2) \int_0^x T_2(\in) d \in -\lambda_2 \int_0^x T_1(\in) d \in + (\beta_2 + \beta_3)\tau_1(x) - \frac{(h_3 + h_2)}{2} \int_0^x \frac{d\epsilon}{\rho(\epsilon)}$$

Considering bending moment equilibrium around the centerline of the solder layer, we could develop an equation that links bending moment to shear stresses.

$$\frac{(h_1 + h_2)}{2} T_1(x) + \frac{(h_2 + h_3)}{2} T_2(x) = \frac{-M}{\rho(x)}$$

$$M = \sum_{i=1}^{3} M_i$$

M_i is the flexural rigidity of the material, which is calculated as,

$M_i = \frac{h_i^3 E_i}{12(1-\gamma_i^2)}$ h- thickness of the material, E –Young modulus, γ-Poisson ratio

The above relationship can be used to simplify the two equations further.

$$(\alpha_2 - \alpha_1)\Delta t x = -\lambda_{12} \int_0^x T_1(\in) d \in + \lambda_2' \int_0^x T_2(\in) d \in + (\beta_2 + \beta_1)\tau_1(x)$$

$$\lambda_{12} = \lambda_1 + \lambda_2 - \frac{(h_1+h_2)^2}{4M}, \lambda_2' = \frac{(h_1+h_2)(h_2+h_3)}{4D} - \lambda_2$$

$$(\alpha_3 - \alpha_2)\Delta t x = -\lambda_{23} \int_0^x T_2(\in) d \in + \lambda_2' \int_0^x T_1(\in) d \in + (\beta_2 + \beta_3)\tau_2(x)$$

$$\lambda_{23} = \lambda_3 + \lambda_2 - \frac{(h_3+h_2)^2}{4M}, \lambda_2' = \frac{(h_1+h_2)(h_2+h_3)}{4M} - \lambda_2$$

The above set of equations were solved in a previous study[142], assuming that shearing stress has a solution in the form of,

$$\tau_i = C_i \sinh kx.$$

Where, k is the eigenvalue of the problem.

In the proposed solution Eigen value k was the solution to the following biquadratic equation.

$$(\beta_1+\beta_2)(\beta_2+\beta_3)k^4-\{(\beta_1+\beta_2)\lambda_{23}+(\beta_3+\beta_2)\lambda_{12}\}k^2+\ \delta=0$$

$$\delta=\lambda_1\lambda_2+\lambda_2\lambda_3+\lambda_3\lambda_1+\lambda_1\frac{(h_2+h_3)^2}{4M}+\lambda_3\frac{(h_2+h_1)^2}{4M}+\lambda_2\left(\frac{(h_2+h_1)}{2\sqrt{M}}+\frac{(h_2+h_3)}{2\sqrt{M}}\right)^2$$

$$C_1=A\left[\lambda_2(\alpha_3-\alpha_1)+\left(\lambda_3+\frac{(h_2+h_3)^2}{4M}\right)(\alpha_1-\alpha_2)-(\frac{(h_2+h_1)(h_2+h_3)}{4M})(\alpha_3-\alpha_2)\right]$$

$$C_2=A\left[\lambda_2(\alpha_3-\alpha_1)+\left(\lambda_3+\frac{(h_2+h_1)^2}{4M}\right)(\alpha_3-\alpha_2)-(\frac{(h_2+h_1)(h_2+h_3)}{4M})(\alpha_2-\alpha_1)\right]$$

$$A=\frac{k\Delta t}{\delta coshkl}$$

$$\lambda_i=\frac{(1-\gamma_i^2)}{E_i}h_i$$

$$\beta_i=\frac{h_i}{3G_i}$$

Where, G_i – shear modulus

Appendix I: Pilot study - 5mm indicator type LED

The 5mm indicator type LEDs were used for the initial pilot study. Commercial InGaN-based white LED package manufactured by Cree Inc. was used for this study. The LED packages were subjected to current stresses of 30mA, 60mA, 90mA and 100mA. The maximum rated continuous current was 30mA and maximum peak current rating was 100mA. The LED packages were of through-hole type. They were attached to a proto-board, and the constant current was provided using a combination of DC power supply and voltage controlled constant current regulator. The LED packages were at 25^0C ambient.

The current-voltage characteristics were extracted periodically till complete failure. The series resistance and ideality factor were extracted from the measured data. The LED packages showed catastrophic failure. It was observed at the failure point there is a bluish glow concentrated around the anode. The LED package showed some resemblance of exponential current-voltage dependence, but it was considered as failure at this point.

The extracted series resistance and ideality factor for an LED package at 60mA is indicated in Figure 68. At the point of failure there is a sharp increase in ideality factor, which indicates that failure is related to die failure. The time to failure also showed power law dependence to current as indicated in Figure 69. These two factors indicate that metal migration have created short-circuit current path between P-GaN and N-GaN regions by-passing the junction. The measured current exponent is quite low for a study that didn't control junction heating. A current exponent that is in excess of 2 was expected, since junction heating would have played a significant role at high currents [56].

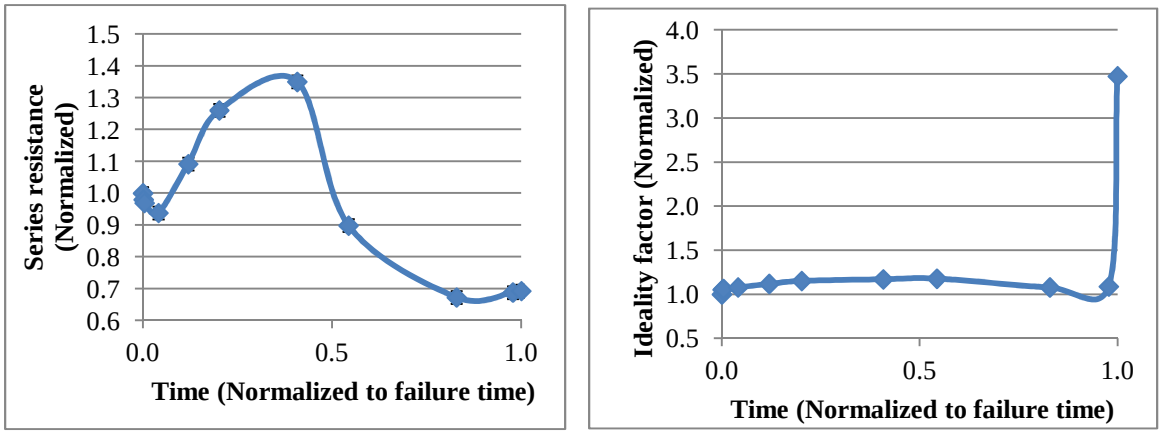

Figure 68. Series resistance and ideality factor change of a 5mm LED package at 60mA

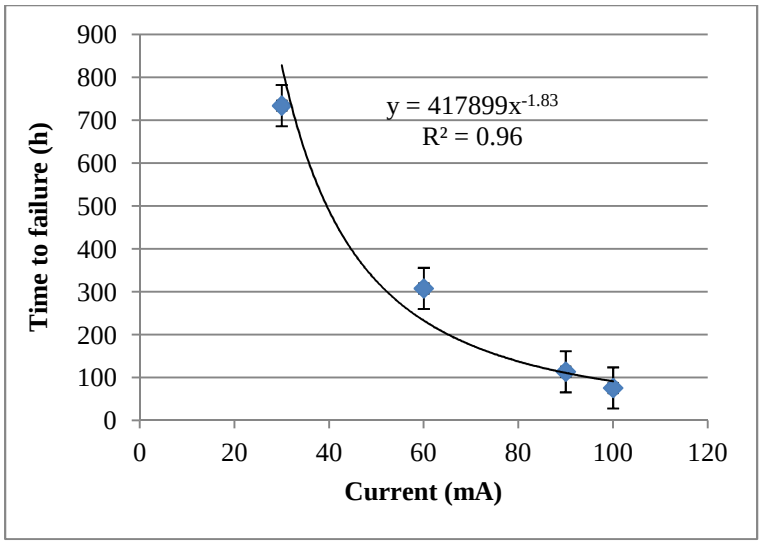

Figure 69. Time to failure at different currents