Area Optimization of a Fast Fourier Transform (FFT) Processor

by

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ABSTRACT

Discrete Fourier Transform (DFT) is one of the most important tools in digital signal processing. It finds application in almost all the cutting edge digital equipments. To effectively compute DFT, Fast Fourier Transform (FFT) algorithms have been devised. Dedicated processor units are employed for these computationally intensive algorithms. The growing demand for everything to be more portable, inexpensive, light-weight and sleek poses a serious challenge for the designer to reduce the size and thus, the cost of the product.

The primary objective of this work is to reduce the area of a 4096-point FFT processor, which currently has a prohibitively large area. This can be done at either the architectural level or the circuit level. First, the processor architecture was decided to be bit-serial, achieving high throughput (~80G symbols per second) and hardware constraints. Next, the critical components (accounting for most area) in the design were identified. After an extensive literature survey, some designs capable of meeting the area requirements were presented. Out of these designs, the ones with the least area were chosen for the critical components (1-bit full-adder and D flip-flop). The components were then designed and tested for performance.

For a signal processing system, the performance metrics are size, power consumption and speed, but this work focuses purely on the area (size) requirements. The work presents significant improvements in the area of the FFT processor. A reduction of 75% was recorded in the sequential part of the circuit, whereas the total area of the processor has been reduced by approximately 40% using this approach. An important point is that the approach followed here is very basic in terms of the modifications made to the circuit. As future work, the scope of the project can be extended if power consumption and speed of the circuit are also taken into account.