A Three-Port Pipelined Register File Implemented Using a SiGe HBT BiCMOS Technology

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The goal of this work is to research, design, test and evaluate a pipelined register file (PRF). A modified version of this register file is also integrated in a test engine with an adder and finite state machine to demonstrate 3D wafer scale integration.

The PRF was implemented using Current Mode Logic (CML) with SiGe heterojunction bipolar transistors (HBT) in two different generations of the BiCMOS technology. The first process features 0.5 µm minimum emitter size HBTs with a cut-off frequency (f_T) of 48 GHz and maximum oscillation frequency (f_{max}) of 69 GHz and the second process features 0.2 µm minimum emitter size HBTs with an f_T of 120 GHz and f_{max} of 100 GHz.

The PRF is composed of three pipeline stages and has one write and two read ports. The PRF includes four 8 word by 32 bit memory banks for the 5DM design and an 8 word by 32 bit memory bank for 7HP design. The register file is designed to operate with an 8 GHz clock for the 5DM design and 16 GHz 7HP design. The estimated power dissipation of PRF is 7W using a 3.4 V voltage supply for the 7HP design.