TRELLIS DETECTOR/DECODER VLSI ARCHITECTURES FOR DATA COMMUNICATION AND STORAGE SYSTEMS

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An Abstract of a Thesis Submitted to the Graduate

Faculty of Rensselaer Polytechnic Institute

in Partial Fulfillment of the

Requirements for the Degree of

DOCTOR OF PHILOSOPHY

Major Subject: Electrical, Computer and Systems Engineering

The original of the complete thesis is on file
in the Rensselaer Polytechnic Institute Library

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March 2007
(For Graduation May 2007)

ABSTRACT

The well-known Viterbi algorithm (VA), and soft-output Viterbi algorithm (SOVA), or maximum a posteriori (MAP) algorithm are widely used for hard-/soft-output trellis detection/decoding in real-life applications. However, all these algorithms involve exhaustive trellis search that makes them essentially not efficient in terms of silicon area and power consumption. Various reduced-complexity trellis detection/decoding schemes have been developed aiming to reduce the silicon area and power consumption. However, despite their great potential for largely reducing computational complexity, their practical application pales in comparison to that of those exhaustive search algorithms. The main reason is that the direct realization of those conventional reduced-complexity algorithms tends to incur a much longer circuit critical path and hence cannot achieve operational throughput comparable to that of those exhaustive search algorithms.

The main contribution of this thesis is the development of algorithm-level techniques to tackle the high-throughput implementation challenge of conventional reduced-complexity algorithms, which will enable numerous real-life applications to exploit their power saving potential. The most widely studied types of reduced-complexity algorithms, including *adaptive* and *reduced-state* trellis detection/decoding algorithms, are considered. In the context of adaptive trellis detection/decoding, conventional algorithms have a global search operation that essentially prevents them from being directly implemented on a high-throughput state-parallel detector/decoder. This work presents a modified adaptive Viterbi algorithm that completely eliminates the global search operation at negligible decoding performance degradation. Using convolutional code decoding as a test vehicle, we demonstrate that the proposed adaptive Viterbi decoder, compared with its state-parallel Viterbi decoder counterpart, can achieve significant power savings and modest silicon area reduction, while maintaining almost the same throughput and decoding performance.

In the context of reduced-state trellis detection/decoding, all the prior work assumes that the trellis reduction is enabled through decision feedback and all the functional blocks in a reduced-state trellis detector/decoder operate on the same reduced-size trellis. Nevertheless, the decision feedback tends to incur a bit throughput penalty and inherently

prevents the use of well-proven high-speed architecture design techniques. We propose a new design approach called quasi-reduced-state trellis detection/decoding. The key idea is to allow different functional blocks operate on differently reduced trellis structures. This will make it possible to completely remove decision feedback, hence largely improve the throughput performance. Meanwhile, the proposed quasi-reduced-state design solution can better match the inherently unequal energy consumption of different functional blocks and realize better design trade-offs among detection performance, power saving, and throughput. The effectiveness of this work has been demonstrated using a soft-output trellis detector in magnetic recording read channel.

Finally, as an attempt to explore innovative application of trellis detection/decoding in data storage, we apply trellis coded modulation (TCM), a widely used technique in data communication, to multilevel Flash memory. We propose to use the concept of TCM to design an on-chip error correction system for Multilevel (ML) Flash memory. Using 2bits/cell Flash memory as a test vehicle, we successfully demonstrate the effectiveness of TCM-based systems, in terms of error-correcting performance, coding redundancy, silicon cost, and operation latency.