A Random-Walk Processing System

by

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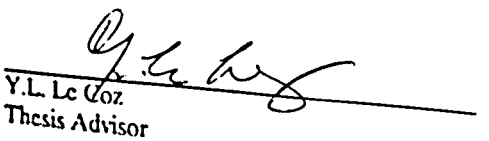

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Abstract

This thesis describes the design of a hardware realization of a random-walk algorithm. A stochastic algorithm for solving any partial differential equation has been implemented in digital hardware with emphasis on speed and efficiency. Maximum computational speed has been achieved through the use of systolic, parallel, and pipelining techniques. The design process began by identifying all algorithmic bottlenecks and then mapping the algorithm onto a suitable architecture. With the basic system laid out, the design was then detailed by specifying the necessary logic elements that would ultimately make up the circuit. Although this design is a dedicated system, the functionality is flexible enough so that it will be applicable to a wide range of problems such as capacitance extraction in complex VLSI geometries or heat flow in objects of varying dimensions such as engine blocks. The computational speed of the random-walk processing system is expected to be Cray-like in ability but at a fraction of the cost.