AN EXPLORATION OF 3D DRAM INTEGRATION AND PROCESS VARIATION

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This thesis focuses on the exploration of 3D DRAM processor integration and process variation.

The memory wall is one of the most significant issues that limit the overall performance of a computer system. Memory wall is the growing disparity of speed between CPU and memory. To deal with the gap between the processor and memory, three-dimension technology is a viable way to achieve better latency and bandwidth of memory. In this work, we conduct a study on 3D DRAM architecture and its integration with multiple processors. Two memory structures are analyzed and then based on them, we introduce the partitioned main memory architecture. This architecture allows non-uniform access to memory to further improve the overall performance. We use the platform with stacking the DRAM main memory on a 4-core processor to evaluate the performance improvement of memory partitioning architecture with two memory structures.

Process variation is also focused on in this thesis. As the feature size decreases, the influence of process variation on circuit is more and more notable. It will affect both the yield and performance of integrated circuits. A large number of processing steps have an impact on critical dimension and thus there are many parameters inducing critical dimension variations. Among them three kinds of variation sources, dose, focus and mask variations are believed to be among most important. We will focus on these three variations in our work. Our work is based on the contours which contain ring oscillators under different process condition. We use the Cadence tools to extract the dimension of each gate in every contour. Through the spectre simulation, the model of ring oscillator delay in terms of gate dimension is built and then used to analyze the spatial variation effect of process parameters.